Efficient Alternate Test Generation for RF Transceiver Architectures

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Efficient Alternate Test Generation for RF Transceiver Architectures

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LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
ATE	Automated Test Equipment
BER	Bit Error Rate
BERT	Bit Error Rate Tester
BIST	Built-in Self-test
BPF	Band-pass Filter
BW	Bandwidth
CDMA	Code Division Multiple Access
CUT	Circuit Under Test
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DIB	Device Interface Board
DSP	Digital Signal Processor
DUT	Design Under Test
EVM	Error Vector Magnitude
FFT	Fast Fourier Transform
GMSK	Gaussian Minimum Shift Keying

GSM	Global System for Mobile
I	In-phase
IC	Integrated Circuit
IF	Intermediate Frequency
IFFT	Inverse Fast Fourier Transform
IIP3	Input third-order Intercept
IMD	Inter-modulation Distortion
ISI	Inter-symbol Interference
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-pass Filter
MARS	Multivariate Adaptive Regression Splines
MSK	Minimum Shift Keying
NF	Noise Figure
OIP3	Output third-order Intercept
OQPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
Q	Quadrature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

RRC	Root Raised Cosine (filter)
SNR	Signal to Noise Ratio
TOI	Third Order Intercept

SUMMARY

The production testing cost of modern wireless communication systems, especially basestation units, is estimated to be as high as 30-40% of their manufacturing cost and is increasing with system complexity, high levels of device integration and scaling of CMOS process technology and operating frequencies. The major production testing challenges for RF transceivers are: (a) the high cost of automated test development because of system-level simulation difficulties and the large simulation times involved, (b) the high cost of using high-end, communication protocol-aware RF test instrumentation, and (c) lack of external test access to RF circuits embedded inside integrated transceivers. Consequently, there exists a need for developing efficient design-for-test methodologies and non-invasive system-level test techniques for wireless transceivers to reduce their test cost. This dissertation is focused towards development of new system-level alternate test methodologies for RF transceiver architectures. The research proposes using non-invasive testing techniques for RF subsystems and digital-compatible built-in testing techniques for baseband and intermediate frequency (IF) analog circuits. The objectives of this research are: (a) to develop automatic test stimulus generation algorithms that allow accurate determination of targeted RF system-level test specification values using behavioral modeling and simulation techniques, (b) to develop RF transceiver test techniques that allow testing of embedded RF systems with limited test access, while reducing the test time for complex RF and baseband system-level performance metrics (b) to significantly reduce the test instrumentation overhead for testing complex frequency-domain and modulation-domain system specifications. The

feasibility and the cost benefits of using the proposed alternate test approaches have been demonstrated using 900 MHz and 1575 MHz transceiver prototypes.

CHAPTER 1

INTRODUCTION

Wireless communication is currently one of the fastest growing areas in the semiconductor industry. Increasing levels of integration and high frequency of operation have made the problem of testing complex radio frequency (RF) transceiver architectures used in wireless communications difficult and cost intensive. Testing transceiver systems is becoming more expensive as the cost of automated test equipment (ATE) having signal handling capability increases rapidly beyond 3 GHz. As these systems incorporate RF components along with analog and digital subsystems, applying a test stimulus signal and measuring the test response signal by means of an external ATE interface are difficult because of the high bandwidth requirements and the adverse effects of parasitics. Moreover, many tests are not amenable to implementation in the manufacturing test procedure because of the test complexity and the long test time. These tests are often restricted to device characterization testing only. The extent of the problem can be gauged by the fact that test cost is approaching approximately 40% of the total manufacturing cost for these systems. In the past, it has been demonstrated that the concept of *alternate testing* can reduce the test complexity and the test cost for the specification-based testing of analog circuits. However, for complex systems under test, as in RF transceivers, the test generation methods used for analog circuits suffer from (1) high simulation complexity, (2) lack of scalability arising from limited test access, and (3) operating frequency limitations. The research findings reported in this thesis extend and implement the concept of alternate testing for the system-level testing

of RF transceiver architectures. This solves the aforementioned limitations of using alternate testing for integrated RF transceiver architectures.

1.1. Production Testing of Wireless Devices and Systems

The major steps involved in manufacturing a wireless system are depicted in Figure 1.1 [1]. At the preliminary stage, application-specific high-level functionalities and product specifications are broadly identified. For example, a communication system using the Code Division Multiple Access (CDMA) ([2], [3]) standard has to abide by the specifications related to the frequency band, the type of modulation, and the RF spectral characteristic requirements set by the corresponding wireless communication standard. Based on these broad-level functionality requirements, a semiconductor vendor or an original equipment manufacturer (OEM) designs the RF transceiver architecture. The transceiver architecture is then divided into multiple functional blocks and their functionalities are distributed over single or multiple integrated circuit (IC) devices based on the production integration capability and the overall performance considerations.

Next, the IC devices corresponding to the system architecture requirements are designed and prototyped by the semiconductor manufacturer. A typical IC design process involves designing the circuit, verifying its specifications using circuit simulation, and fabricating prototype devices. Characterization measurements are performed on these prototype ICs using a test-bench instrumentation to verify the device performance over a range of physical and electrical parameters, such as frequency, ambient temperature, supply voltage, signal power, loading conditions, etc. The characterization data is used for redesigning the prototype devices to improve the design performance, if necessary. Also, the characterization

data serves as a reference point for production testing in the subsequent high-volume manufacturing stage.

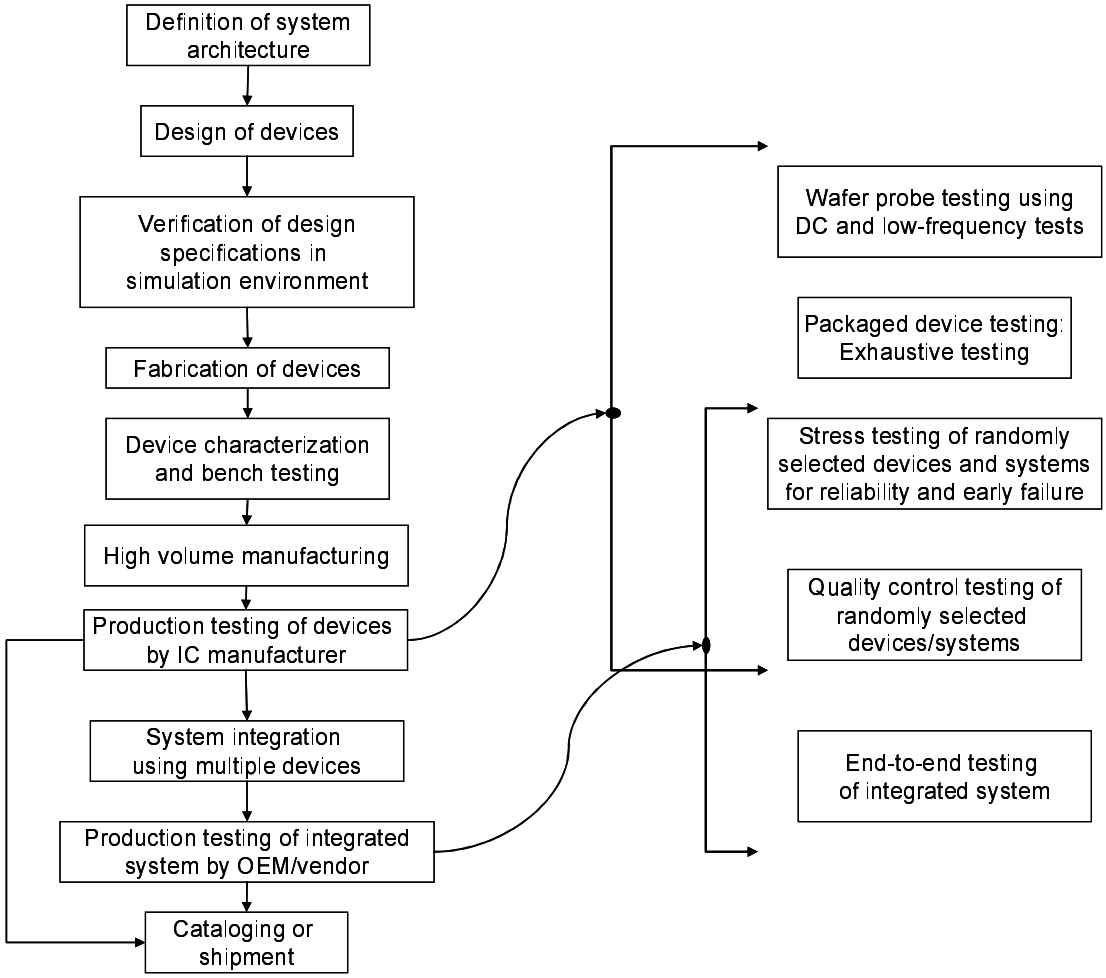

Figure 1.1. Various stages of manufacturing of a wireless system.

Production testing comes into play after the high-volume manufacturing of these devices [4]. Production testing consists of wafer sort testing on automatic test equipment (ATE) connected to a wafer prober, followed by packaged device testing on an ATE connected to a handler. Besides wafer probing and handler testing, a randomly selected set of devices is used to perform stress testing at elevated temperatures for testing the early failure and reliability of the ICs. Furthermore, exhaustive quality control tests are performed on randomly selected

devices throughout the production lifetime for an IC or system design. Next, these devices are integrated into the RF transceiver system by the semiconductor vendor or the OEM. End-to-end system-level production tests are performed on these systems before cataloging or shipping them to customers.

The primary objective of production testing is to identify and reject the devices or systems that either fail functionally or do not meet all of the required specifications in the early stages of production. Since the cost of production testing increases the final cost of the shipped devices or systems without adding any further performance benefit, minimizing the cost of production testing is of prime importance in test engineering [5].

1.2. Cost of Production Testing for Wireless Devices and Systems

Figure 1.2 shows a typical production testing setup for a device in production [1]. The device-under-test (DUT) is placed on a test socket located on the load board or the device interface board (DIB). The DIB routes the signal from an ATE test-head to the socket pins via signal traces and relays. A DIB may also contain additional testing circuitry that is necessary to test the DUT. ATE instrumentation resources connect to the test-head through high-bandwidth cables. In general, for testing a specification or a functionality of the DUT, one or more test instrumentations are programmed to send test stimulus waveforms to the DUT inputs and to capture the test response waveforms from the DUT outputs. The test response waveforms are analyzed to verify the DUT functionality or to compute the specifications of interest. Test control software is another essential part of the production testing system. It allows high-level programming of the test hardware instrumentation;

sequencing a series of tests; storing the high-volume test stimulus and test response data; and efficiently analyzing, displaying, and reporting the test data and results.

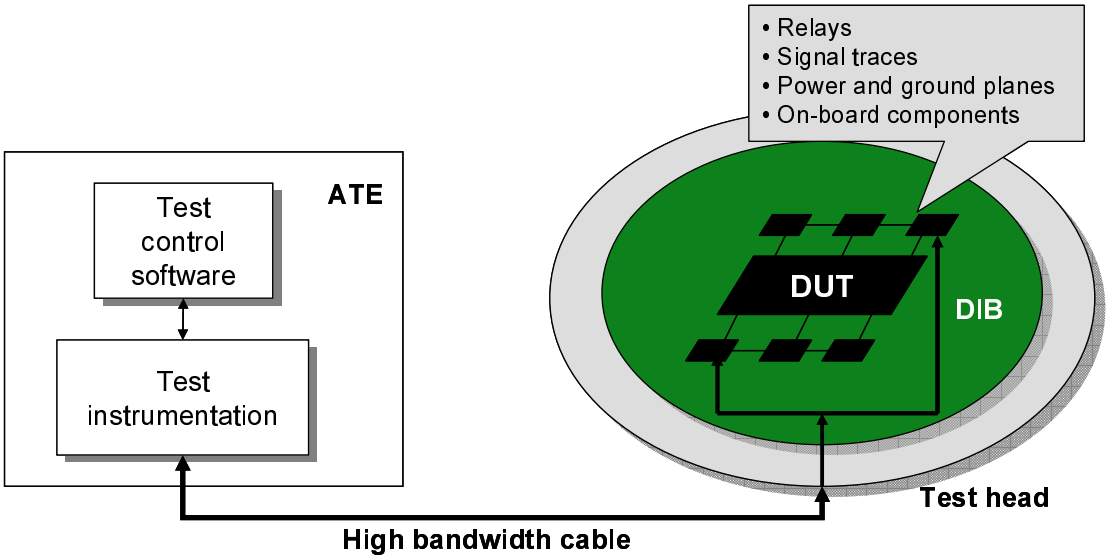

Figure 1.2. A typical production testing setup.

Figure 1.3 shows the key parameters in a production testing setup, which determines the test quality and the cost of testing [1]. These parameters are as follows:

- Measurement accuracy of the ATE instrument
- Measurement precision or repeatability for a given test setup
- Dynamic range of signal handling of the ATE instrumentation
- Repeatability of measurements across multiple ATEs
- Measurement delays in the form of test signal settling time and signal round-trip delays in the test-data pipeline
- Time required for programming the ATE instruments and switching the relays
- Signal limitations because of socket, cable, and DIB parasitics
- Noise in the measurement setup

- Maximum speed or frequency at which the test signals can be applied and captured
- Requirement of protocol awareness implemented into the ATEs for complex system-level specification testing
- Test controllability and test response observability of the internal nodes of a system-under-test

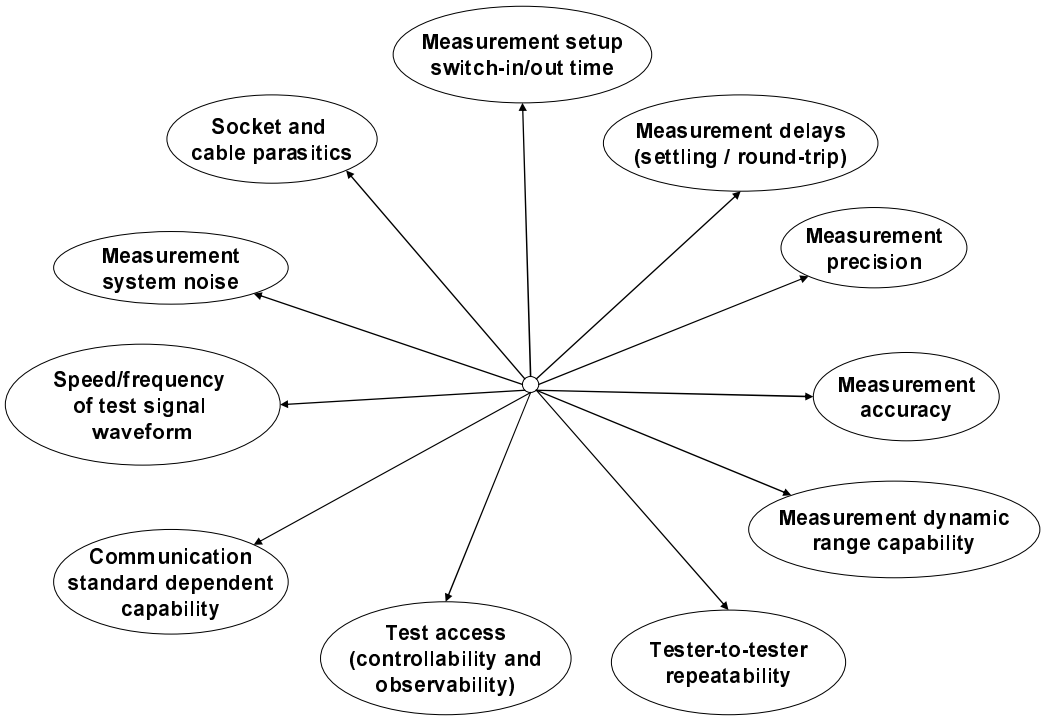

Figure 1.3. Key measurement parameters determining the cost and the accuracy in a production testing setup.

A typical wireless transceiver consists of various digital, analog, mixed-signal, and RF submodules [6]. The functional blocks internal to a typical mobile hand-held set are shown in Figure 1.4. The specifications of these sub-modules and the entire system vary widely in nature. In general, the production testing of complex mixed-signal and RF systems requires communication protocol-aware, expensive RF ATE to exhaustively test an end-to-end wireless transceiver system [7].

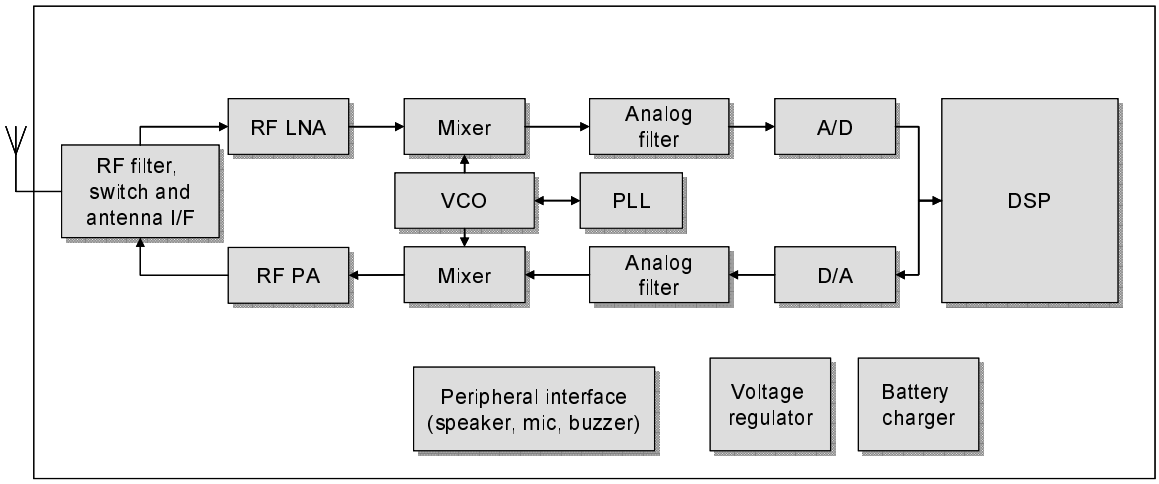

Figure 1.4. Digital, analog, mixed-signal and RF components in a typical mobile hand-held wireless system.

Given the wide range of functionalities integrated into a single system, no single method exists to reduce the testing time or to improve the testing accuracy for all possible specification tests. Recently, the complexity and the range of problems associated with the production testing of wireless systems have drawn much research interest. An overview of the reported research work is provided in the following section.

1.3. Previous Work

In the semiconductor industry, the state of the art in the manufacturing testing of RF transceiver architectures has been to break down the problem into several smaller problems by testing individual components or subsystems separately. For example, testing baseband DSP is done primarily by means of the IEEE 1149.1 boundary scan [8]; testing analog subsystems is done by means of inserting additional test accesses around it ([9], [10]).

However, for testing embedded RF components, putting additional test accesses is not favored because of the adverse effect of these access points on impedance matching [11].

In the research community, there have been efforts to develop designs-for-testability hardware, which can be embedded on-chip for making some of the RF measurements. The work presented in [12] measures the spectral content of the test response using the direct down-conversion of RF test stimuli and test response waveforms. Although the chip area taken by additional test circuitry is of concern, it shows the feasibility of using a built-in test for measuring the performance of high-frequency embedded analog/RF blocks in-situ. The authors of [13] - [15] have developed a subsampling-based digitizer that can be used for capturing narrow-band RF waveforms. On the other hand, in [16], the authors attempt to extend their delta-sigma modulator-based built-in self-test (BIST) approach for measuring signal-to-noise ratio (SNR), frequency response, and intermodulation effects for wireless communication devices. In [17], the authors have proposed, in a conceptual manner, using a dedicated down-conversion path on the same chip for down-converting the transmitter output back to baseband. At the same time, by means of an RF coupler, the authors propose feeding the transmitter output back into the receiver input. However, the concept presented has been supported by no experimental data in [17]. The author of [18] presents a way of measuring the s-parameter for wideband RF channels. In [19] and [20], the authors have used a defect-oriented testing approach and the corresponding concept of fault coverage in test automation for testing Bluetooth transceivers. For system-level baseband specifications, such as BER ([21], [22]) and EVM ([23], [24]), analyses pertaining to different data modulation schemes have been analyzed in the past. An accelerated measurement technique has been tried for lowering the test time for digital datalinks ([25]-[27]). However, from the manufacturing test point of view, these system-level tests have remained expensive because of the prolonged test time required.

Alternate testing also has been applied to perform specification testing of RF components and circuits in the past. In [28], the authors attempted to alleviate the problem of bandwidth limitation of ATE cable by designing a modulator (which up-converts the low-frequency test signal sent from ATE) and a demodulator (which down-converts the RF test response in low frequency) on the DUT load-board. The down-converted test response is used as a test signature of the DUT for predicting its specifications. In [29], the authors investigated different characterizing features of the test response spectra of a low-noise amplifier after comparing it with a white noise signal. The extracted test response features would correspond to the specifications of the RF component under test and can be used to predict the specifications of the RF components. In [30], the author attempted to replace the need for using high-frequency testing by alternately monitoring the transient change in the bias current of an RF time-domain multiplexing access (TDMA) power amplifier, and the information contained in such changes in bias current is measured to be reflective of DUT specifications, such as adjacent channel power ratio (ACPR) [31].

Although, the above-mentioned alternate testing approaches have been investigated for RF components and circuits, the feasibility of using alternate testing procedures at the system level has been explored only recently ([32], [33]). The research work reported in this thesis falls under such a system-level approach and aims to develop an alternate test framework for RF transceiver architectures. The basic concept of alternate testing is described in the following section.

1.4. Alternate Testing: Basic Concepts

Past research work in the area of automated test generation for analog circuits ([34]-[41]) showed that the variation of any process or circuit parameter, such as width of a FET, value of a resistor, etc., in the process or circuit parameter space ***P*** affects the circuit specification ***S*** by a corresponding sensitivity factor. The variation in these parameters also affects the measurement data in the measurement space ***M*** (for example, the sampled DUT response waveform captured by an ATE digitizer or the amplitude spectrum of a DUT response captured by spectrum analyzer) of the circuit by a corresponding sensitivity factor. Figure 1.5 illustrates the effect of varying one such parameter in ***P*** on the specification ***S*** and the corresponding variation of a particular measurement data in ***M***. For any point in p in the parameter space ***P***, a nonlinear mapping function onto the specification space ***S***, f:***P***→***S***, can be computed. Similarly, for the same point p in ***P***, another nonlinear mapping function onto the measurement space in ***M***, f:***P***→***M***, can be computed. Therefore, for a region of acceptance in the circuit specification space ***S***, there exists a corresponding allowable region of variation of parameters in the parameter space ***P***. This in turn defines a region of acceptance of the measurement data in the space ***M***. A circuit can be declared faulty if the measurement data lies outside the acceptance region in ***M***.

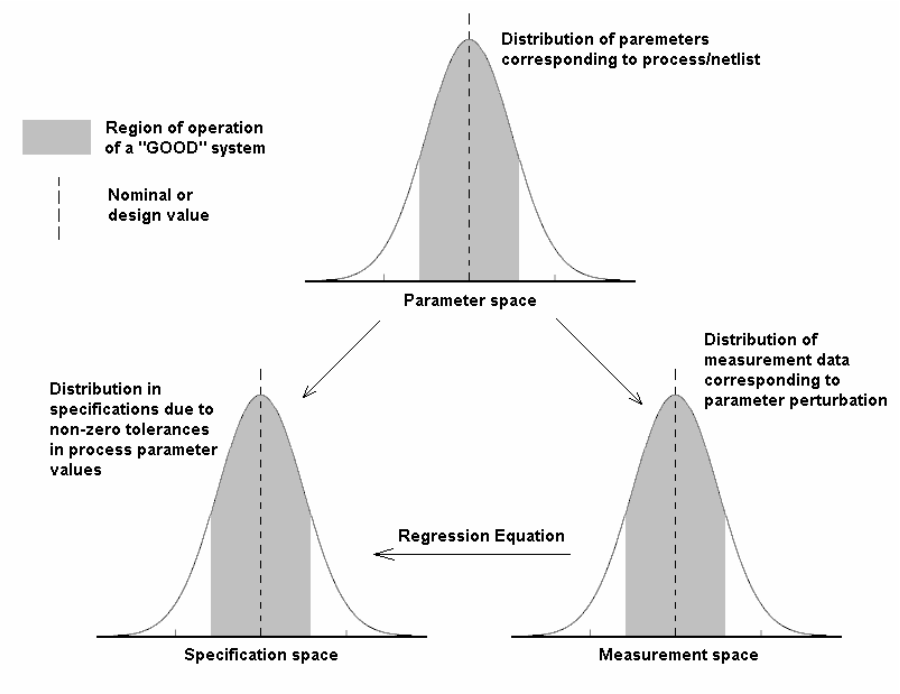

Figure 1.5. Variation in process or circuit or behavioral parameter and its effect on specification space and measurement space.

Alternatively, [34]-[38] showed that a mapping function $f: \boldsymbol{M} \rightarrow \boldsymbol{S}$ could be constructed for the circuit specifications $\boldsymbol{S}$ from all the measurements in the measurement space $\boldsymbol{M}$ using nonlinear statistical multivariate regression. Given the existence of the regression model for $\boldsymbol{S}$, an unknown specification of a system-under-test can be predicted using the measured data. The objective of automated test selection in the alternate test paradigm is

- to select a simple test stimulus such that test instrumentation and test access overheads are simplified,
- to predict circuit specifications accurately from the alternate test response such that no faulty DUT is determined as acceptable, or vice versa, resulting in classification error.

In this research, alternate tests have been applied to accelerate the production testing and to simplify the complexity of the production test hardware needed for the specification

testing of RF transceiver architectures. An overview of various types of modern RF transceivers is given in the following section.

1.5. Overview of Wireless Transceiver Architectures

A zero-IF or direct conversion system ([42], [43]) is conceptually the simplest type of architecture (Figure 1.6 and Figure 1.8). The baseband message bandwidth spans from DC to a certain frequency (Figure 1.7) determined by the baseband digital data rate. The quadrature modulation is done at RF [43]. In practice, the performance of a zero-IF transceiver largely suffers from the following:

- Spurious signals falling onto the DC because of second-order intermodulation distortion (IMD) effects and local oscillator (LO) leakage. These spurious signals are difficult to filter away in DSP as the DC is included within the message bandwidth itself.
- Flicker noise spectral density at near-DC frequencies getting integrated over the baseband low-pass filter bandwidth.

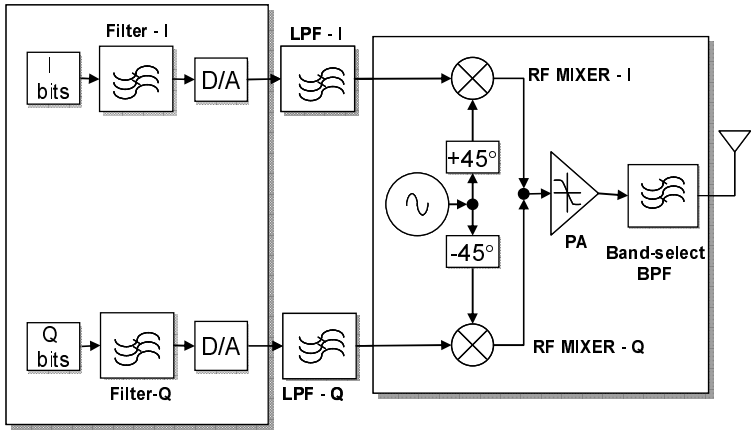

Figure 1.6. Zero-IF (direct conversion) wireless transmitter.

Figure 1.7. Message spectrum at the transmitter output for zero-IF systems

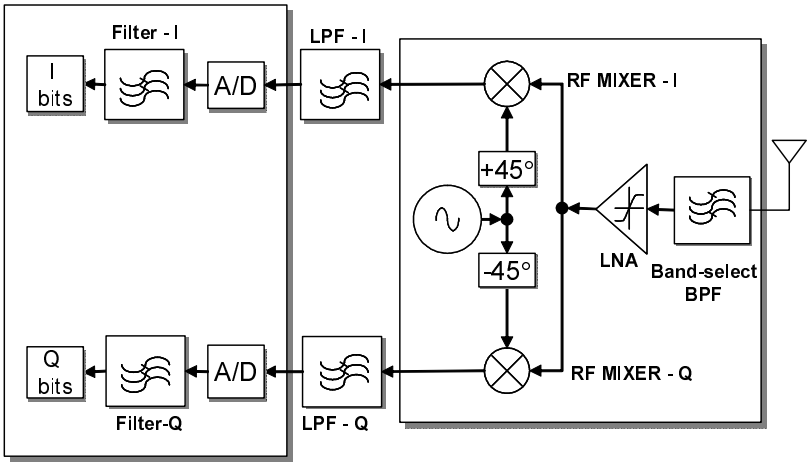

Figure 1.8. Zero-IF (direct conversion) wireless receiver.

The low-IF architectures (Figure 1.9 and Figure 1.11) take advantage of implementing digital (de)modulation at IF within their DSP [43]. At the same time, the quadrature mixing of I and Q signals is done at RF to suppress one of the upper and lower side-bands to increase the RF bandwidth efficiency. Flicker noise and second-order intermodulation effects at near-DC frequencies are effectively eliminated by the IF band-pass filter. Figure 1.10 shows the message spectra at baseband, IF and RF.

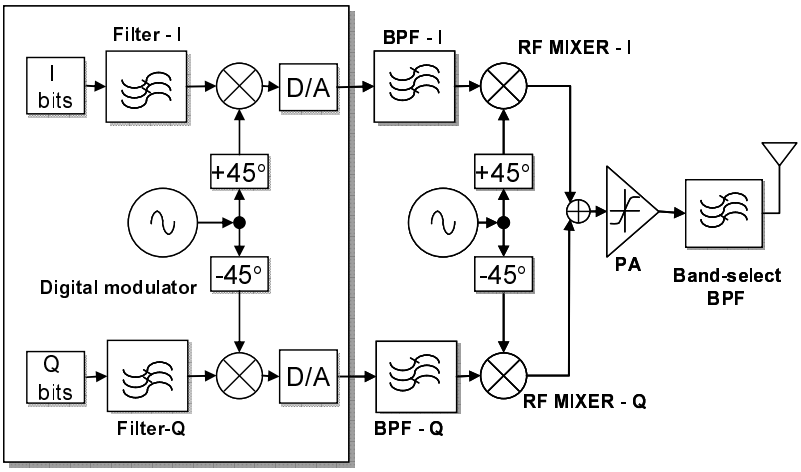

Figure 1.9. Low-IF wireless transmitter with RF quadrature mixing.

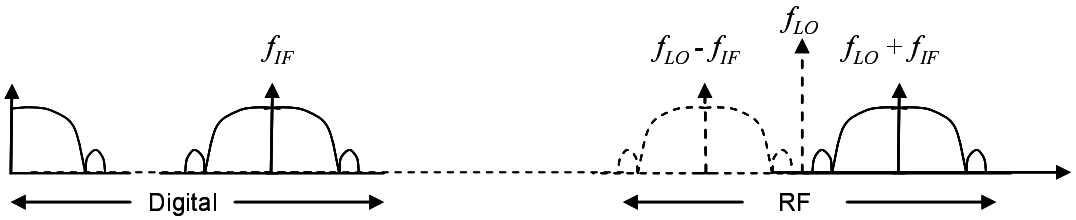

Figure 1.10. Message spectrum at the transmitter output for low-IF systems.

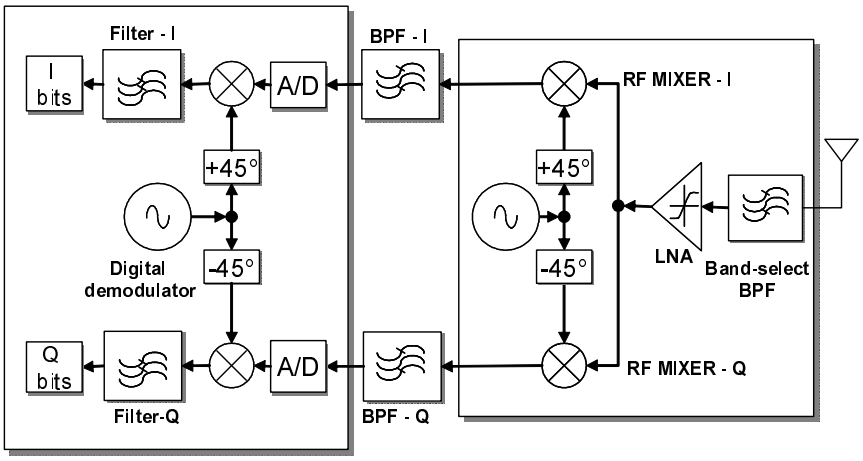

Figure 1.11. Low-IF wireless receiver with RF quadrature mixing.

The low-IF digital receiver (transmitter) may also use a simple down-conversion (up-conversion) scheme (Figure 1.12 and Figure 1.14). Because of the absence of the RF quadrature carrier, the LO frequency synthesis for up-conversion and down-conversion mixing is simpler than the previous two architectures. However, the efficient suppression of one of the upper and lower side-bands (Figure 1.13) requires band-pass filters of high quality (Q) factor.

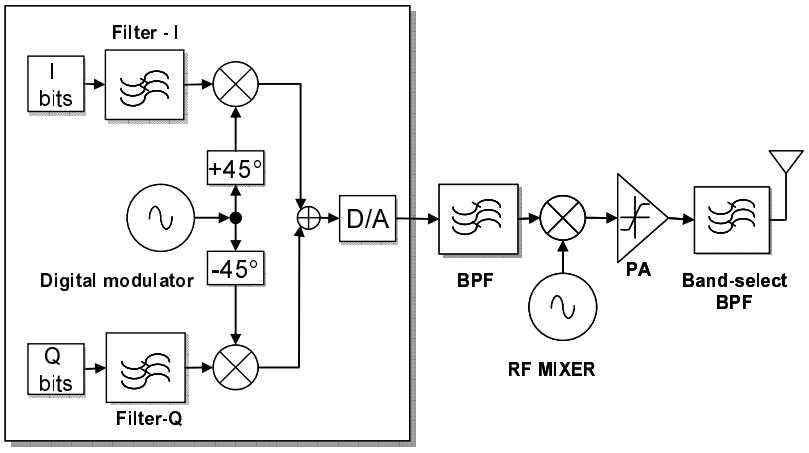

Figure 1.12. Low-IF wireless receiver using simple (non-quadrature) RF up-conversion.

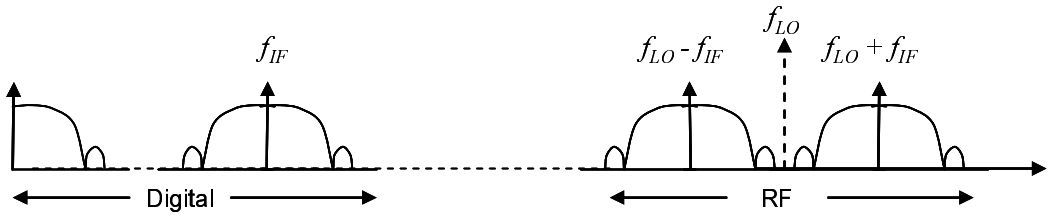

Figure 1.13. Message spectrum at the transmitter output for low-IF systems with simple (non-quadrature) up-conversion.

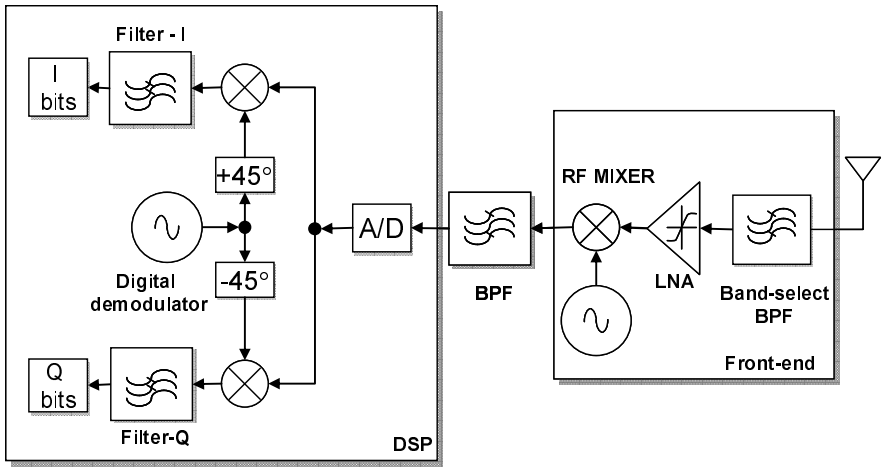

Figure 1.14. Low-IF wireless receiver using simple RF down-conversion.

It should be noted that, irrespective of the various underlying configurations used in realizing an RF transceiver, the end-to-end specification testing requirements do not change. However, the design-for-testability (DfT) approaches using built-in test hardware are affected by the various system architectures.

1.6. Research Contributions

The objective of the research reported in this thesis is to develop low-cost production testing solutions for specification testing the RF front-end; the baseband and IF analog interfaces, and the end-to-end transmitters and receivers using alternate testing methodology. The key tasks of this research are as follows:

1. A digital compatible testing approach for the analog interface circuits in baseband and IF (Chapter 2).
2. A multitone testing framework for the receiver RF front-ends (Chapter 3). This work proposes behavioral simulation-based fast automated test generation for RF subsystems.
3. A low-cost production testing framework for end-to-end specification testing of the RF receivers. Modulation-domain specifications (e.g. EVM) and frequency-domain specifications (e.g. gain, nonlinearity, noise figure) are tested simultaneously applying a single test (Chapter 4).
4. A low-cost multitone testing framework for testing modulation-domain and frequency-domain end-to-end specifications of the RF transmitters (Chapter 5).

5. A loopback testing approach for testing the gain and the nonlinearity of the transmit and the receive subsystems of an RF transceiver using an optimized modulated bit sequence (Chapter 6).
6. A diagnostic technique for detecting catastrophic failures (shorts and opens in signal traces) on the device interface boards (Appendix A).

Hardware measurements are presented for 900 MHz and 1.575 GHz RF transceiver prototypes. In summary, the research work presented in this thesis is a step toward lowering the highly prohibitive production testing cost for RF transceivers used in gigahertz wireless systems.

In summary, the primary contribution of this research is as follows:

- The presented work is the first to successfully demonstrate the concept of alternate testing methodology at the system-level for end-to-end system specification testing. It solves the system-level test generation scalability problem existing in the simulation-intensive automated (alternate) test generation.
- The presented work is the first to perform end-to-end system specification testing for RF transceiver systems using simple analog test stimuli for which lengthy digital bit-sequences are traditionally used. The outcome is a significant reduction in overall testing time and the simplification of the test-hardware architecture needed for testing the complex, system-level specifications.

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CHAPTER 2

SPECFICATION TESTING OF BASEBAND AND IF ANALOG CIRCUITS

In this chapter, the proposed alternate test techniques for baseband and intermediate frequency (IF) analog circuits, e.g. IF filters and amplifiers, are discussed. An automated concurrent multitone test stimulus generation and test point selection approach is presented. Also, a digital compatible test response observation approach is described in this chapter. It should be noted that A/D and D/A interfaces are built into any RF transceiver system. However, the conversion speed of the on-chip A/Ds is often limited to voice-band signal. To compensate for the low sampling rate and to improve the digital filtering performance, the baseband DSP interpolates the sampled voice-band signal using sinc interpolation techniques [1]. The digital compatible approach provides a low-cost way to sample the analog test response of analog filters operating in the intermediate frequency range.

2.1. Previous Work

Various approaches exist in analog and mixed-signal testing to ensure the desired operation of analog circuit-under-test (CUT). One approach, for example, models the catastrophic failure modes ([2] - [4]) of analog CUT, where the analog circuit fails to operate correctly because of internal shorts, opens, and other manufacturing defects and this approach uses corresponding tests for detecting these defects [5]. On the other hand, in testing

approaches using parametric failure models [6], where one or more specifications of the circuit deviate from the respective design values because of random variations in the manufacturing process, specification-oriented tests (SPOTs [7]) are used. SPOTs compute the specifications of analog CUT and compare them with respective specification acceptance limits to make pass-fail decisions during production testing. Different fault models and corresponding test approaches have been proposed in the literature ([3]-[5], [8]-[12]) to detect catastrophic failures using defect-oriented-testing (DOT [7]) and parametric failures in SPOT.

In this chapter, a new specification-oriented test approach is presented that aims to accurately test the specifications of analog circuits under parametric (multi-parameter) failure conditions. The proposed test approach uses the concept of alternate testing for the specification testing of analog circuits introduced by [13] and [14]. In alternate testing, the circuit specifications are computed (predicted) using multivariate nonlinear regression analysis of the test response waveforms under process and circuit parameter variations. In the proposed test approach, the analog CUT is stimulated with DC and large-signal multitone waveforms under parametric failure conditions, i.e. multi-parameter circuit/process perturbations. The test response waveforms at one or more circuit nodes are observed and the circuit specifications are predicted using statistical regression models. The key aspects of the proposed approach are as follows:

An automated test point selection and test optimization approach for accurately predicting the analog CUT specifications. The efficiency of this approach lies in determining critical parametric failure modes, followed by concurrent test-point selection and multitone test stimulus generation using a fast, greedy algorithm that minimizes the specification prediction error of alternate tests.

A digital-compatible method has been developed for accurately capturing the analog test response of embedded analog circuits in the absence of fast, high-resolution A/D converters so that the specification tests can be performed accurately. The response capture technique uses vernier digitization schemes introduced in [15]. In the proposed work, it is integrated with the IEEE 1149.1 scan architecture, which is commonly used for a testing digital core.

Hence, the primary objective of the proposed approach is to maximize the accuracy of the SPOT in terms of multitone test generation by means of efficient test response observation using test point selection and test response waveform digitization technique. In contrast to the test point selection approach reported earlier [9], where the controllability and the observability are maximized, the proposed approach maximizes the accuracy of the specification test (specification prediction) using the alternate test paradigm. In a similar way, the objective of the test generation approach is different from the other multi-frequency test generation approaches in [8], [10], and [12], where the fault coverage under a fault model is maximized.

2.2. Basic Concepts of Alternate Testing

The specifications of analog circuits-under-test, as explained in the literature ([13], [14], [16]), vary because of the variation of process and design parameters. The variation of any process or circuit parameter, such as the width of a FET, value of a resistor, etc., in the process or circuit parameter space $\boldsymbol{P}$ affects the circuit specification $\boldsymbol{S}$ by a corresponding sensitivity factor. Let $\boldsymbol{M}$ be the space of measurements (e.g. sampled values of test response waveform) made on the circuit-under-test; the variation in the parameters also affects the measurement data in the measurement space $\boldsymbol{M}$ of the circuit by a corresponding sensitivity

factor. Figure 2.1 shows the variation in one such parameter in ***P*** resulting in a corresponding variation in specification in ***S*** and variation of a particular measurement data in ***M***. Given the parameter space ***P***, for any point in ***P***, a nonlinear mapping function onto the specification space ***S***, $f:\boldsymbol{P}\rightarrow\boldsymbol{S}$, can be computed. Similarly, for the same point in ***P***, another nonlinear mapping function onto the measurement space in ***M***, $f:\boldsymbol{P}\rightarrow\boldsymbol{M}$, can be computed. Hence, for a region of acceptance in the circuit specification space, there exists a corresponding acceptance region in the parameter space. In turn, it defines a region of acceptance of the measurement data in ***M***. A circuit is said to be faulty if the measurement data lies outside the acceptance region in ***M***.

Alternatively, [13], [14], and [17] demonstrated that a mapping function $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$ can be constructed for the circuit specifications ***S*** from all the measurements in ***M*** using nonlinear multivariate regression. Given the existence of the regression model representing $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$, an unknown specification of a CUT can be predicted from the measured test response data.

In alternate test methodology, a specially crafted stimulus is used, such that the regression function $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$ is accurately constructed for predicting the specifications of the CUT under process variations. The objective of the proposed test approach is to synthesize the measurement space ***M*** to construct regression models for the accurate prediction of any circuit specification ***S***. However, the primary problems involved in such an approach are as follows:

- The requirement of repetitive simulations of the CUT under parametric variations for test optimization and large size of the circuit and process parameter space of the analog CUT results in high simulation cost for automated test generation.

- For a measurement space consisting of sampled test response waveforms, the accuracy of predicting specification using regression models, f:M→S, is affected by the A/D resolution on a production tester.

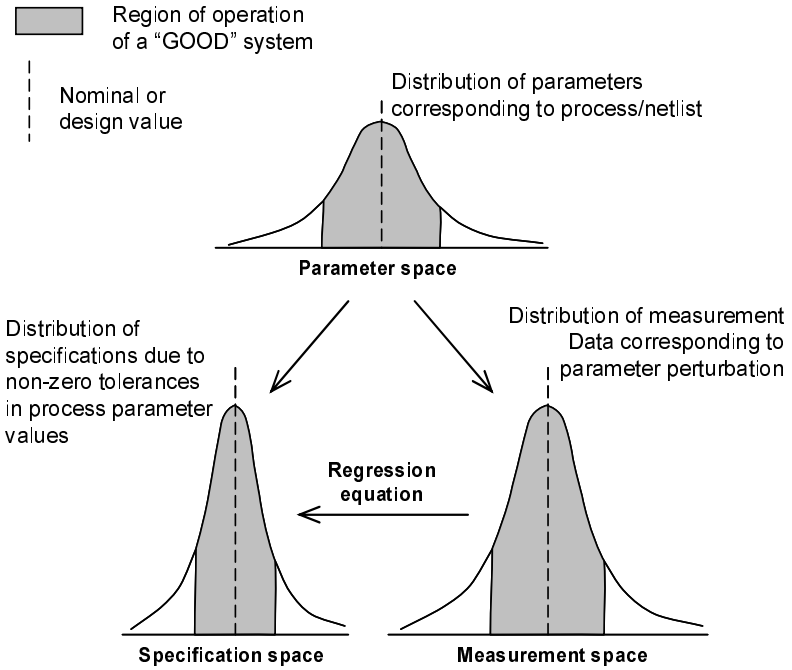


Figure 2.1. Effect of variation in process or circuit parameter on CUT specification and test response measurement.

In the proposed approach, the specification testing of embedded analog CUT is performed by:

1. modeling the parameter space and selecting critical (multi-parameter) perturbation modes in the parameter space,
2. selecting test response observation points to increase the accuracy of specification predicting regression models and optimizing the test stimulus signal using critical perturbation modes, and

3. using a subsampling-based data acquisition approach to capture the analog test response waveforms of analog CUT embedded in the system in the absence of high-resolution A/Ds.

Multivariate Adaptive Regression Splines (MARS) [18] are used to construct the regression model and estimate the test specifications of analog CUTs from the test response waveforms.

2.3. Test Architecture

The test architecture relies on the application of a multitone test stimulus designed to maximize the ability to predict the circuit-under-test specifications from the observed test response measurements (Figure 2.2). For test stimulus application, an analog multiplexer is used to apply the test stimulus in test mode. The test stimuli are applied externally by a mixed-signal ATE. For simple test stimuli (e.g. single-tone), they may be generated internally by an on-chip voltage-controlled oscillator, hence, trading off chip-area for ATE dependency. The test response waveforms are observed by the external ATE at one or more circuit nodes in the test mode.

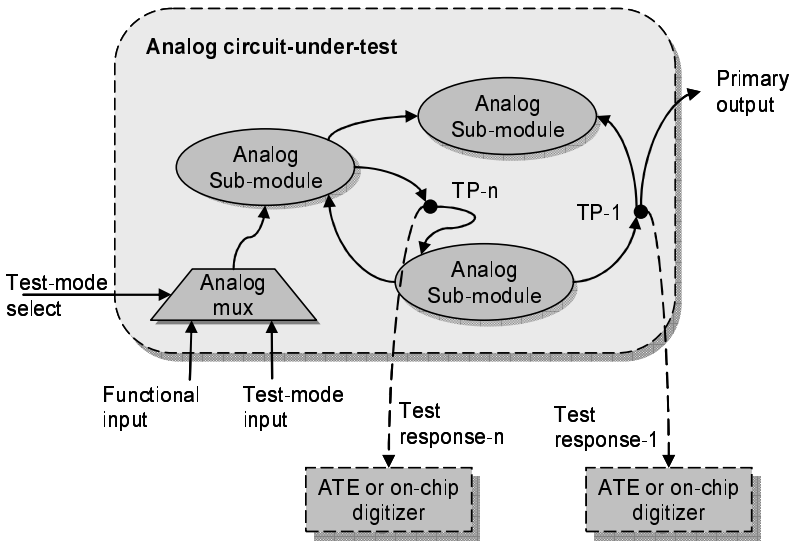


Figure 2.2. Test architecture for test response observation.

For an analog CUT embedded into larger systems, the parasitics of ATE cable, the limitation of A/D conversion speed (in samples/sec), and limited resolution (in number of bits) of the ATE digitizer lead to the inaccurate capture of the analog test response waveform. In the proposed method, a vernier technique-based digitization scheme introduced in [15] is employed. In the proposed method, the digitization scheme is integrated with the scan architecture of the digital core. The principle of vernier digitization is as follows.

To digitize a voltage value at any specific time point *t* of the test response waveform, that value must be compared with various other appropriately selected reference voltage levels. The results of these comparisons determine the corresponding digitized data with some quantization error. For example, in an *n* bit A/D converter, there are (2^n-1) such comparison levels. In the vernier digitization technique [15], the comparison of the CUT test response at time *t* against all possible voltage levels of the reference waveform is achieved by applying many cycles of the periodic stimulus waveform to the CUT and a reference waveform to a comparator input. The test response waveform and the reference waveform

repeat with different cycle lengths, which is analogous to the well-known vernier measurement technique used to measure a fraction of space units. Figure 2.11 illustrates this principle (for an analog filter circuit) by showing that at each successive cycle of test response waveform, a sampled voltage value of the waveform is compared with different reference voltage levels appearing at the comparator input. The comparison process occurs for a prescribed number of cycles, depending on the required digitization accuracy in terms of lowering the quantization error. The longer the comparison cycles, the lower the quantization error. In the proposed approach also, as shown in [15], a low-cost reference waveform generator using a switched capacitor RC circuit is configured for digitizing the analog test response waveform (Figure 2.11(b)). The comparison voltage levels of the reference waveform are generated by feeding a pulse train to the switched capacitor RC circuit. Assuming that the pulse train is generated by dividing the system clock by $2N$ using a counter, the reference waveform value on the n^{th} clock is given by:

$$V(n) = \begin{cases} V_{DD}\left[1 - \dfrac{\alpha^{n}}{1+\alpha^{N}}\right]; 0 \le n < N \\ V_{DD}\dfrac{\alpha^{(n-N)}}{1+\alpha^{N}}; N \le n < 2N, \text{where } \alpha = \left(1 + C_{SW}/C_{O}\right)^{-1} \end{cases} \quad \textbf{(2.1)}$$

where, C_{SW} = the switching capacitor value, and

C_O = the value of the output capacitor of the reference waveform generator circuit.

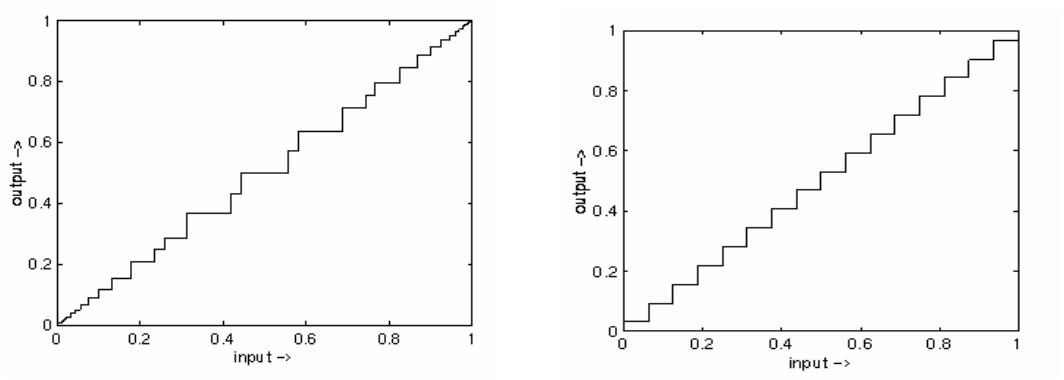
Since a closed form analytical expression for all the quantization steps can not be derived because of the mixing of voltage levels from two different equations, the quantization steps are obtained numerically. Table 2.1 shows the dynamic ranges and the maximum and minimum values of the quantization steps for different choices of α and N. *V-High* and *V-Low* are the upper and lower bounds of the voltage swing of the reference waveform. The

columns next to *Max step-size* and *Min step-size* show the number of bits required by an ADC with linear characteristics for the given step sizes.

Table 2.1. Dynamic ranges and quantization steps with the reference waveforms (normalized to VDD).

α	*N*	V-High	V-Low	Dynamic range	Max step-size	Eqv. # ADC bit	Min step-size	Eqv. # ADC bit
0.75	16	0.9901	0.0099	0.9802	0.1138	3.1060	0.0033	8.2110
	32	0.9999	0.0001	0.9998	0.1249	3.0010	3.3481e-005	14.8660
	64	1.0000	0.0000	1.0000	0.1250	3.0000	3.3636e-009	28.1474
0.9	16	0.8437	0.1563	0.6873	0.0498	3.7863	0.0019	8.5073
	32	0.9668	0.0332	0.9336	0.0416	4.4875	7.2349e-004	10.3336
	64	0.9988	0.0012	0.9976	0.0445	4.4856	1.3085e-004	12.8964
0.95	16	0.6944	0.3056	0.3888	0.0230	4.0771	0.0017	7.8352
	32	0.8377	0.1623	0.6754	0.0219	4.9451	6.5136e-004	10.0182
	64	0.9638	0.0362	0.9277	0.0223	5.3768	2.1504e-004	12.0748

Using the *2N* quantization levels of the reference waveform, response period *N´* and (*2N* x *N´*) comparison results, one can identify all the *N´* reference voltage pairs within which the corresponding analog response samples lie. The mid-values of the *N´* voltage pairs represent the reconstructed quantized test response waveform sampled at system-clock speed. Any sample that is above or below the dynamic range of the reference waveform range is approximated to *V-High* and *V-Low*. Figure 2.3 shows the input-output relationship of the proposed test response waveform extraction method in contrast to an ADC with linear transfer characteristics. Figure 2.4 shows the nature of the respective quantization errors. A circuit response lying relatively within the upper or the lower region of the dynamic range of the reference waveform, where quantization error is less, is desirable. Appropriate test stimuli may be selected to meet this criterion.



(a) (b)

Figure 2.3. (a) ADC characteristics using the reference waveform (α=0.75,N=16); (b) linear ADC characteristics (4 bit).

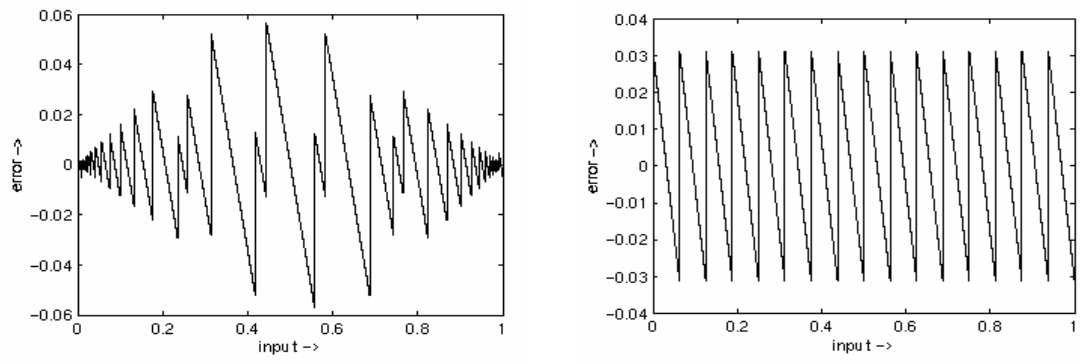


Figure 2.4. Quantization error (a) for the reference waveform (α=0.75,N=16); (b) for the linear ADC (4 bit).

The advantages of using the above reference waveform generation technique are that (a) the reference waveform generation circuitry is simple, and (b) if α is the ratio of the two capacitances of Equation (2.1), the reference waveform generator is immune to process variations that affect the individual capacitance values (since the two capacitors values track each other keeping their ratio relatively constant). For N>>1, the fractional change in reference voltage resulting from the changes in capacitor values can be expressed as

$$\frac{\Delta V(n)}{V(n)} \propto \frac{\frac{\Delta C_{SW}}{C_{SW}} - \frac{\Delta C_{O}}{C_{O}}}{1 + \frac{C_{O}}{C_{SW}}} \tag{2.2}$$

Equation (2.2) shows that, for unidirectional variation of the component values, the effect of the changes in one capacitance will tend to cancel the effect of the changes in the other. The other advantage of using switched capacitor circuits is that at the time of voltage comparison by the comparator and the subsequent latching action of the register, the voltage at the reference (negative) input of the comparator is static. The voltage at the comparator reference input always changes in the other half-cycle of the clock when the comparator output is not latched.

Hence, for a suitable choice of the reference waveform, each sample of the test response waveform is compared with *2N* different reference voltage levels. The resulting bit sequence at the output of the comparator, representing all comparison results, is fed to the scan chain of the digital core, as shown in Figure 2.5. Using the knowledge of the reference waveform, the analog test response waveform is reconstructed in the ATE and is used for predicting specification of the CUT under process/circuit parameter variations. In reality, the speed of operation of the proposed subsampling-based digitization technique is limited by the accuracy and the speed of the sample-and-hold operation (which needs to run at a faster system clock-rate) of the comparator input circuitry, rather than the accuracy of the reference waveform (which needs to run at divide-by-2N clock rate).

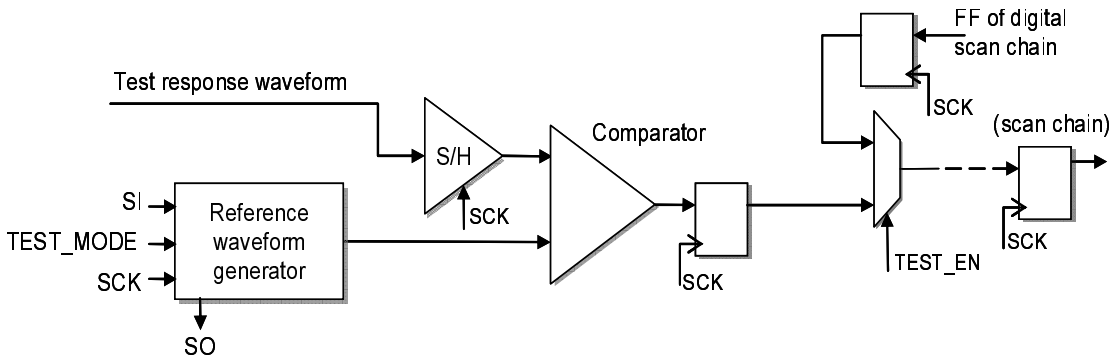


Figure 2.5. On-chip hardware for digitization and capturing analog waveform using a scheme compatible with IEEE 1149.1.

2.4. Test Generation Approach and Algorithms

The test stimulus consists of DC and sinusoidal multitones (large signal). The test stimulus and the test response observation points are selected efficiently using an automated process, which is described in this section. The core test generation approach consists of the following steps:

1. Identify critical single-parameter and dual-parameter perturbations that have the maximum contribution to the (nonlinear) effect on circuit specifications. To reduce the simulation complexity, the relationship is assumed to be restricted to second-order nonlinearity between the parameter perturbations and the corresponding variations in specification values.
2. Perform a simultaneous dual search for the optimal set of test frequencies and test points, for a specified number (input to the algorithm) of test points using transfer function characteristics at different candidate test nodes around the analog CUT's DC bias. Simulations for iterative test stimulus optimization are large signal for both linear and

nonlinear circuits. The relative fitness of the candidate test stimulus waveforms is determined by simulation using the critical process perturbations determined in step 1.

After selecting the test stimulus, compute the accurate regression model using rigorous multi-parameter perturbations. This step incurs one-time simulation cost, as opposed to the repetitive simulations required in step 2.

2.4.1. Computing Critical Parameter Perturbations

Specification failures resulting from parametric deviations are modeled in terms of the parameters and their tolerances as follows [19]. Let $\boldsymbol{P}$ be the collection of N process and circuit parameters for an analog CUT, denoted by the set $\{P_{10}, P_{20}, \ldots, P_{N0}\}$ representing the nominal values of the parameters. The statistical distribution of each parameter and its correlation coefficient with respect to the distribution of every other parameter in $\boldsymbol{P}$ is known from prior wafer test structure measurements. In the absence of the above data, each parameter in $\boldsymbol{P}$ is assumed to vary independently (i.e. no two parameters are correlated). This represents the worst case scenario of all possible independent perturbation modes in the parameter space. If x_i represents the percentage deviation of the parameter P_i corresponding to its $\pm 3\sigma$ deviation from its mean, then $P_i \in [(P_{i0} - x_i P_{i0}), (P_{i0} + x_i P_{i0})]$. The normalized deviation for P_i is given by $p_i = (P_i - P_{i0}) / x_i P_{i0}$; where, $p_i \in [-1, 1]$, for all $i=1 \ldots N$ and $P_i \neq 0$.

On the other hand, if, S_0 is the design value of the specification, the normalized deviation s is given by $s = (S - S_0) / S_0$. Assuming that the specification limits are two-sided, *i.e.* the specification has both the upper and lower limits, normalized limits s_u and s_l can be computed

as: $s_h = (S_H - S_0) / S_0$, and $s_l = (S_0 - S_L) / S_0$. The normalized deviation in specification is modeled as:

$$\mathbf{s} = \mathbf{A}\, p^T + p\, \mathbf{B}\, p^T + p\, \mathbf{C}\, p^T \qquad \textbf{(2.3)}$$

where, $\mathbf{A} = \{a_1, a_2, \ldots, a_N\}$, $\mathbf{B} = \mathrm{diag}(\{b_1, b_2, \ldots, b_N\})$, and

$$C = \begin{Bmatrix} 0 & C_{12} & C_{13} & \cdots & C_{1N} \\ 0 & 0 & C_{23} & \cdots & C_{2N} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & 0 & \cdots & C_{N-1,N} \\ 0 & 0 & 0 & \cdots & 0 \end{Bmatrix}.$$

The elements a_i's ***A*** and b_i's in ***B*** are computed using circuit simulation, where the parameter P_i is perturbed keeping other parameters at their respective nominal values and s is computed for each perturbation (Figure 2.6 (a)-(b)). The a_i and b_i are computed by fitting the quadratic regression curve $s = a_i p_i + b_i p_i^2$ in Equation (2.3).

A specification S is considered insensitive to a parameter variation in P_i, if

$$|a_i| \le \alpha \min (s_u, s_l) \text{ , i=1... N} \qquad \textbf{(2.4)}$$

where, the threshold value α is a constant, $0 < \alpha < 1$. The higher the value of α, the more sensitive is the specification to parametric perturbation model.

After ***A*** and ***B*** are computed, the circuit is simulated using the joint parameter perturbations of the parameter pair (P_i, P_j), while keeping other parameters at their respective nominal values and computing s each time (Figure 2.6(c)). The c_{ij}'s in ***C*** are computed by fitting the linear regression curve $s - (a_i p_i + b_i p_i^2 + a_j p_j + b_j p_j^2) = c_{ij}(p_i p_j)$ of Equation (2.3).

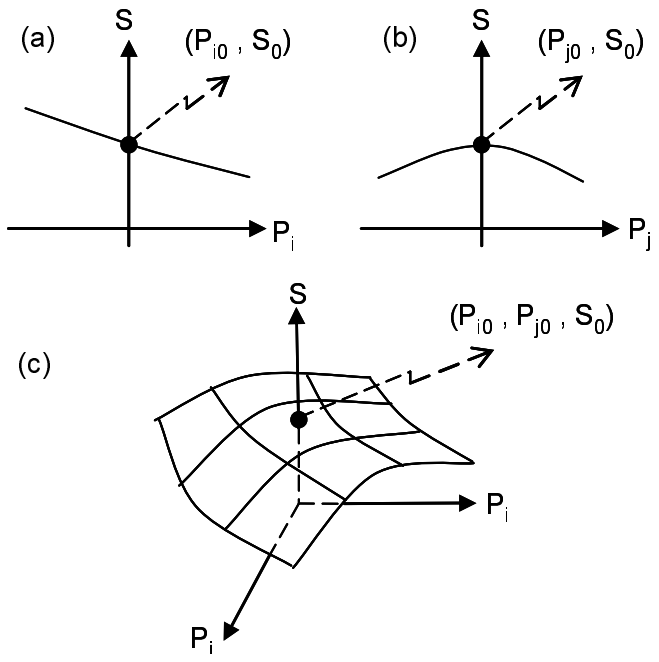


Figure 2.6. Effect of (a, b) single and (c) joint parameter perturbations on circuit specification.

Since the parametric deviations in the model are normalized w.r.t. their worst case tolerance values, the computed coefficients in $\boldsymbol{A}$ (or $\boldsymbol{B}$ or $\boldsymbol{C}$) are directly compared with each other to find the relative importance of the parameter deviations in terms of how they affect the circuit specifications. The sensitivity-based analysis presented in [6] corresponds to the particular case of $\boldsymbol{B}\equiv\mathbf{0}$ and $\boldsymbol{C}\equiv\mathbf{[0]}$ in the present analysis. The assumption of $\boldsymbol{B}\equiv\mathbf{0}$ and $\boldsymbol{C}\equiv\mathbf{[0]}$ is less accurate for modeling parameters such as device mismatch, where any deviation in either the +ve or-ve direction from the nominal value exhibits a decrease (or increase) in the specification value, as shown in Figure 2.6(b). The slope of the sensitivity of the circuit specification to the parameter value around the nominal parameter value, however, is zero or small. The computation of $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ is simulation intensive, but it incurs a one-time simulation cost.

Any iterative algorithm-based test generation scheme requires that the CUT be simulated repeatedly. The simulation cost is high if **A**, **B**, and **C** have a large number of coefficients. Therefore, to reduce the simulation cost during test stimulus generation, a subset of parameter perturbations (of all the prior simulated parameter perturbation modes) is selected for use during test generation and is based on the relative values of the coefficients in **A**, **B** and **C**. The specification S of the CUT is therefore relatively more susceptible to the selected critical parameter perturbations than to others. More specifically, a single or joint perturbation mode in the parameter space **P** is said to be critical for the accurate computation of the specification in a specification based test if the following are satisfied:

$$|a_i| \geq \beta \min\left(s_u, s_l\right), i=1 \ldots N \quad \textbf{(2.5)}$$

$$|b_i|, |c_{ij}| \geq \gamma \min\left(s_u, s_l\right), \text{i=1} \ldots \text{N} \quad \textbf{(2.6)}$$

The higher the value of β, the less parameter sensitive the fault model, whereas the higher the value of γ, the more linearized the fault model. For multiple specifications, the overall set of critical perturbation modes consists of the union of the individual critical perturbation modes (sets of perturbations) for each of the specifications.

2.4.2. Test Generation and Test Point Selection Algorithm

The goal of the test generation algorithm is to determine the best multi-sine test stimulus waveform and a set of test response observation points and corresponding response measurements from which the CUT test specifications can be predicted as accurately as possible (see Figure 2.1). The core test generation algorithm consists of the following steps:

1. Preliminary small signal AC simulation and sensitivity analysis to determine an initial choice of test points and test frequencies.

2. The large-signal transient AC simulation of candidate test waveforms to handle nonlinear circuits during test stimulus generation.

A multitone sinusoidal waveform is the transient test stimulus of choice. The test stimulus $X(t)$ is of the form:

$$X(t) = V_0 + \sum_{m}^{N_m} u(t - t_{0m}).V_m \sin\left(w_m (t - t_{0m})\right) \qquad \textbf{(2.7)}$$

where,

V_0 = overall DC offset,

V_m = amplitude for m-th tone,

t_{0m} = initial delay for m-th tone,

N_m = maximum number of tones to be present in $X(t)$.

The selection of the test waveform parameters and the concurrent selection of test response observation points is performed by the algorithm discussed below.

For each critical perturbation mode $\boldsymbol{P}_k$, at each circuit node n, the frequency response of the CUT, $\Delta H_k(jw)$'s, are computed using AC simulation, where, $\Delta H_k(jw, n) = H_k(jw, n) - H(jw, n)$, $H_k(jw,n)$ = amplitude response for single or joint perturbation $\boldsymbol{P}_k$, (small signal analysis for nonlinear circuits), and $H(jw, n)$ = amplitude response for nominal parameter values in $\boldsymbol{P}$ (small-signal analysis for nonlinear circuits) at a circuit node n.

At the circuit node n, for a test-response frequency w, the observability vector for all the critical perturbation modes from the parameter set $\boldsymbol{p}$ is defined as:

$$\mathbf{O}(n,w) = [\Delta H_1(jw,n)\ \ \Delta H_2(jw,n)\ \ldots\ \ \Delta H_k(jw,n)\ \ldots]$$

The higher the value of $||\mathbf{O}(n,w)||$, the more sensitive the test-response waveform of frequency w at the given node n to all the critical perturbations. The candidate test response observation point and the candidate test stimulus frequencies are chosen such that $||\mathbf{O}(n,w)||$'s are large and $\mathbf{O}(n,w)$'s have an orthogonal relationship with each other as follows:

1. For the given set of critical parameter perturbation modes and the test response frequency w, a circuit node n_1 is a better candidate than the circuit node n_2 for being selected as a test-response observation point, if $\|\mathbf{O}(n_1,w)\| > \|\mathbf{O}(n_2,w)\|$.
2. For the given set of critical parameter perturbation modes and circuit node n, the test response frequency w_1 is a better selection than w_2, if $\|\mathbf{O}(n,w_1)\| > \|\mathbf{O}(n,w_2)\|$.

Based on (1) and (2), once an observability vector $\mathbf{O}(n_1, w_1)$ is selected, the selection criterion is extended over multiple test points and test response frequencies. The vector $\mathbf{O}(n_2, w_2)$ is deemed a better candidate than $\mathbf{O}(n_3, w_3)$ when used along with $\mathbf{O}(n_1, w_1)$ for test generation, if

$$\frac{\left\|\hat{O}(n_1, w_1).\hat{O}(n_2, w_2)\right\|}{\left\|O(n_1, w_1)\right\|.\left\|O(n_2, w_2)\right\|} < \frac{\left\|\hat{O}(n_1, w_1).\hat{O}(n_3, w_3)\right\|}{\left\|O(n_1, w_1)\right\|.\left\|O(n_3, w_3)\right\|}$$

, where $\hat{O}(n,w)$ is the unit vector in the direction of $\mathbf{O}(n,w)$. Hence, the more orthogonal the observability vector to $\mathbf{O}(n_1, w_1)$ is, the better chance it has to be combined with $\mathbf{O}(n_1, w_1)$ during test generation.

Applying the criteria in (1) to (2), a list of candidate test points and associated test-stimulus frequencies is obtained. A fast, greedy algorithm is used for the final selection of the number of frequencies. In this algorithm, *large-signal* simulation is performed for both linear and nonlinear circuits [19].

The search for the minimum prediction error implemented in the algorithm is a fast, greedy search and may converge to a local minimum. However, sinusoids with new frequencies are included in $X(t)$ in successive iterations to achieve lower specification prediction error. In contrast to other test point selection approaches, such as [11], where the test point selection approach attempts to maximize the controllability and observability, in the proposed approach, the final test observation points are selected in conjunction with the test generation algorithm attempts to increase the accuracy of the test using an iterative search technique. It should also be noted that, during test stimulus optimization in step 2, the

sampled waveform is used as the measurement space (Section 2.2). For an embedded analog CUT, the analog waveform that is digitized using the subsampling-based technique (Section 2.3) is used as the sampled waveform data.

2.4.3. Computing Regression Models for Specification Prediction

After test stimulus and test point selection, the regression models for specification prediction are recomputed using rigorous multi-parameter perturbation that includes both critical and non-critical parameter perturbations. Unlike for the test stimulus optimization step 2, which requires repetitive circuit simulation, the simulation cost in this step is one-time. Consequently, in this step, the selected test stimulus remains unchanged, but the accuracy of the regression models, $f: \boldsymbol{M} \rightarrow \boldsymbol{S}$ (Section 2.2), is increased since non-critical parameter perturbations, which are left out during test stimulus optimization, are also included. The resulting regression models are used, in conjunction with the test stimulus obtained in step 2, for predicting the specifications of analog circuits.

BEGIN Test Stimulus Generation and Test Point Selection Algorithm:

selected test-points:= the first candidate test-point in the list

do begin

frequency list {w_m's} in Equation (2.7):= the first frequency in the list for the given test-points

do begin

initialize [V_0, {V_m, t_{0m}}'s] of Equation (2.7) as

$V_0 := 0;\ t_{0m} := 0;\ V_m := (V_{DD} - V_{SS}) / (2 * N_m)$

do begin

Simulate netlist for all critical perturbation vectors

*Create statistical regression model representing f:**M**→**S**, where,*

***M** is the test-response waveforms at the selected test points*

Simulate netlist for a set of random perturbation vectors

*Compute specification, evaluate f:**M**→**S** and compute their difference (error in spec. prediction) for the random perturbation vectors*

error = max (absolute values of prediction errors)

Select another [V_0, {V_m, t_{0m}}'s] in its vicinity based error values in previous iterations using the following constraints:

$V_{SS} < V_m,\ V_0 < V_{DD}\ ;\ 0 < t_{0m} < 2\pi / w_m$

***while**(local minimum for error is found);*

if**(error < input-error-threshold) **then

***break** outer loop;*

else

include another frequency from the list

end

***while** (no. of frequencies test stimulus < N_m)*

include another test point from the list

***until**(all candidate test points are utilized)*

END

2.5. Experimental Results

In this section, case studies for which the proposed test generation and test point selection method has been applied are presented.

Case study I: The first example is a low-pass leapfrog filter [20]. The circuit component values are: R_1= R_2= R_3= R_4= R_5= R_6= R_7= R_8= R_9= R_{10}= R_{11}= 10kΩ; C_1= C_4= 10nF; C_2= C_3= 20nF (Figure 2.12(a)). The op-amps are assumed to be fault free in this example. The tolerance is assumed to be 10% around the nominal value of the resistors and the capacitors. In the circuit performance metric space, the -3 dB bandwidth of the filter is chosen as the specification of interest. The circuit is fault free if the cut-off frequency lies within 1.4 kHz ± 100 Hz. In the presented examples, a 1 Msamples/s 12-bit DAC model having [-5V, 5V] output dynamic range has been used for the applying transient stimulus to the CUT.

The test generation and test point selection approach is verified by injecting parametric failures in the form of random variations of the components around their nominal values. The specifications for these circuits are predicted with the regression model and pass/fail decisions are made. The predicted 3dB bandwidth specifications are compared with the -3 dB bandwidth specification information available from AC analysis. The predicted values exhibit close agreement with the specifications obtained from AC analysis and all of the predicted specification data lie in the vicinity of the straight line with slope +1, which represents the locus of "ideal" predictions. When using single test response observation point 'vout' (the primary output), the proposed approach is able to distinguish between faulty and fault-free circuits if the actual bandwidth specification values do not lie within the prediction error of ±2.9% around the upper and lower limits of the acceptance region in the test

specification. For two test points selected (primary output and one optimal internal test point), the above prediction error reduces to ±1.9%. The results are summarized in Table 2.2.

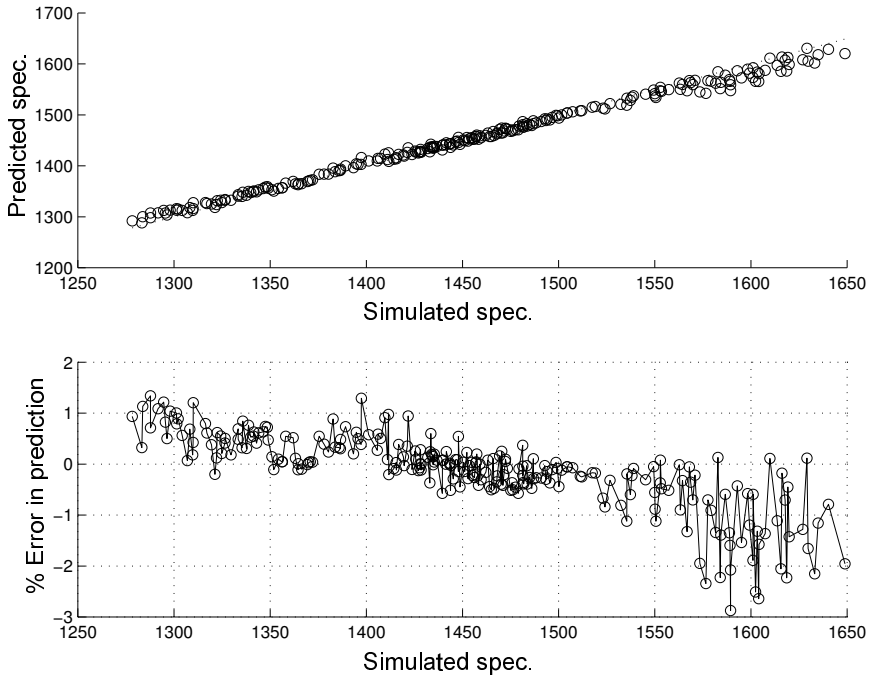


Figure 2.7. Prediction of the 3-dB bandwidth specification of Leapfrog filter; single test-point = 'vout'; (a) prediction tracking (b) prediction error < 2.9%.

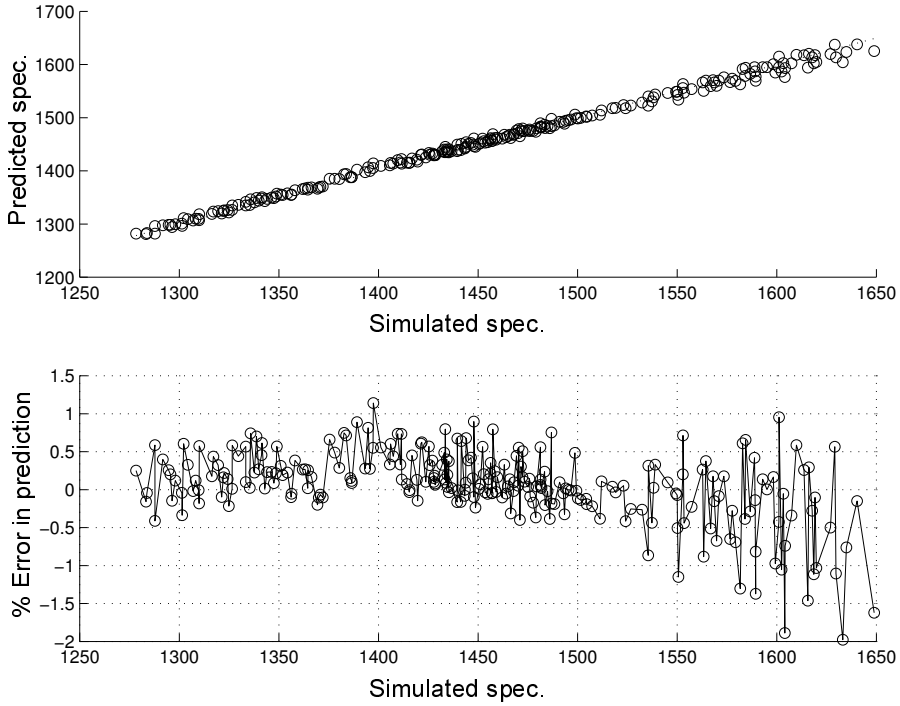
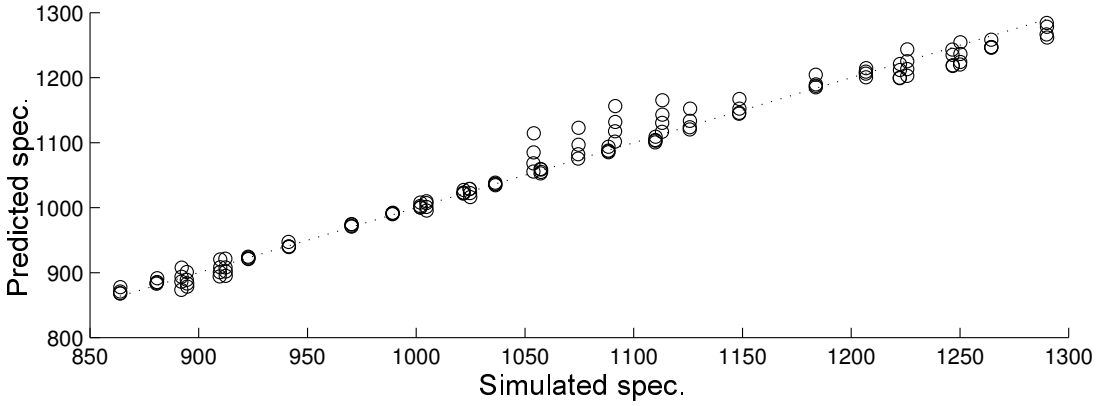


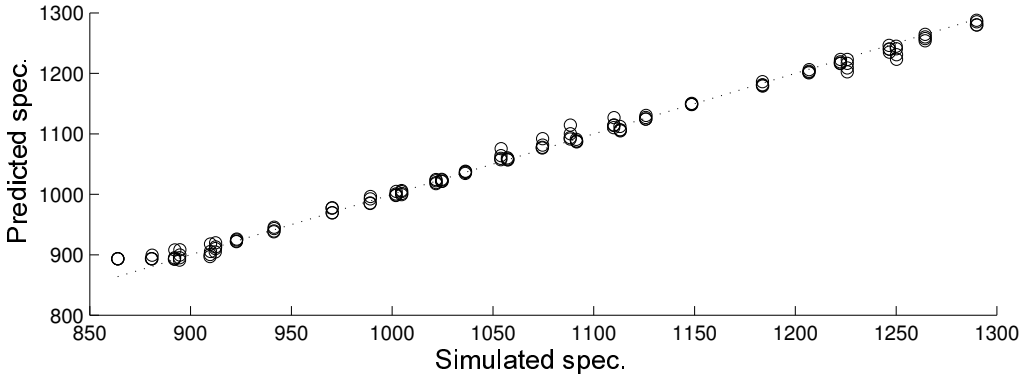
Figure 2.8. Prediction of the 3-dB bandwidth specification of Leapfrog filter; 2 optimal test-points '10' and 'vout'; (a) prediction tracking (b) prediction error < 1.9%.

Case study II: The second example is a continuous-time state-variable filter [15]. The circuit component values are: R_1= R_2= R_3= R_4= R_5= R_6= 10kΩ, R_7 = 12kΩ; C_1= C_2= 20nF (Figure 2.12(b)). The -3 dB cut-off frequencies of the high-pass and low-pass functions and the center frequency of the band-pass function were selected as the specification of interest. The nominal specification values are 610 Hz, 1.07 kHz and 800 Hz, respectively. The circuit is said to be fault free if the frequency specifications lie within ± 100 Hz of the respective nominal values. In Figure 2.9 and Figure 2.10, the tracking of the -3 dB low-pass cut-off frequency and band-pass center frequency are shown as examples. While selecting the optimal single test response observation point, the band-pass function output node was selected by the test generation algorithm. However, for selecting two optimal test points for

the same specifications, the low-pass and high-pass function output nodes were picked by the algorithm. Test accuracy improves for a greater number of optimal test points selected. The results presented are for single-tone (N_m = 1) test stimulus waveforms with non-zero DC offset.

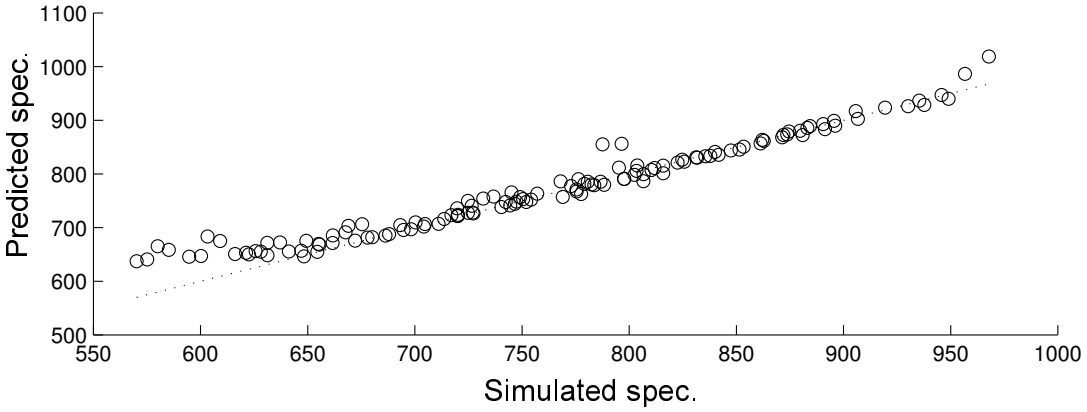


(a)

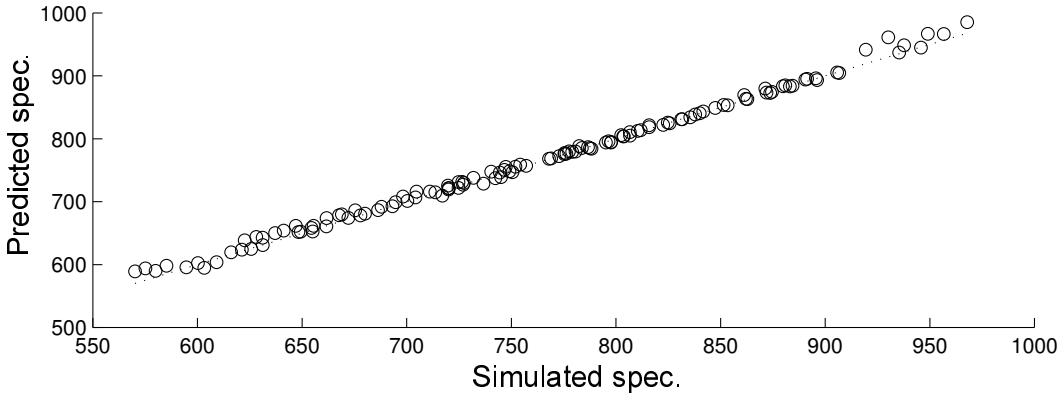


(b)

Figure 2.9. Low-pass 3dB cut-off frequency specification tracking for state-variable filter; (a) 1 optimal test point 'bp_vout', prediction error < 4.2%; (b) 2 optimal test-points 'lp_vout' and 'hp_vout', prediction error < 2.0%.



(a)

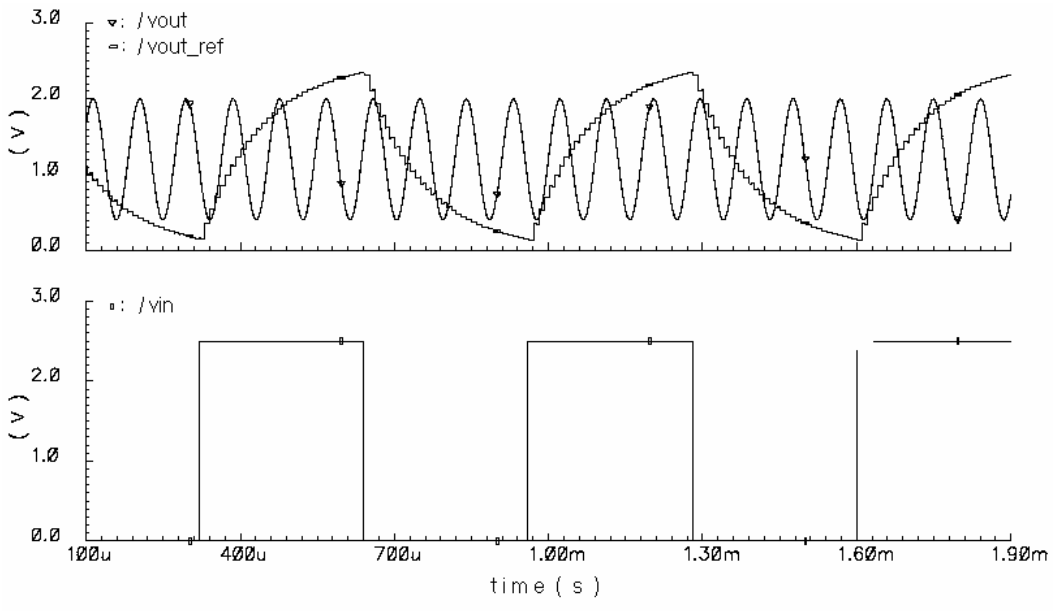


(b)

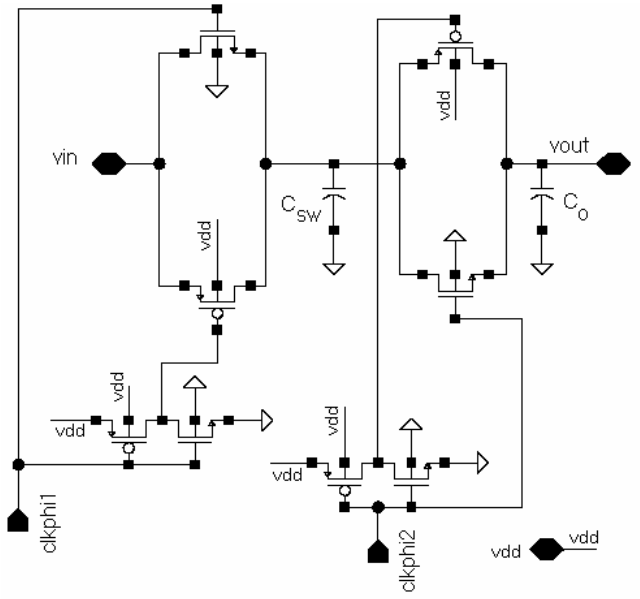
Figure 2.10. Band-pass center frequency specification tracking for state-variable filter; (a) 1 optimal test point 'bp_vout', prediction error < 5.8%; (b) 2 optimal test-points 'lp_vout' and 'hp_vout', prediction error < 2.1%.

Case study III: In the next example, a second-order Tow-Thomas band-pass filter is used. The center frequency and the gain at center frequency were selected for the specification test. The nominal specification values are 10 kHz and 0 dB. The circuit component values are: R_1= R_2= R_3= R_4=15.92kΩ, R_5= R_6= 10kΩ; C_1= C_2= 1nF (Figure 2.12(c)). Specification acceptance limits of ±1 kHz and ±1 dB were selected. In this example, vernier digitization was applied to capture the test response waveform as a digital bit

sequence. A single-tone test stimulus is selected by the test generation algorithm and the primary output node is selected for test response observation. The test response waveform (at 11 kHz) is compared with a reference waveform for vernier scheme based digitization. The reference waveform was generated using a switched-capacitor RC circuit (Figure 2.11(b)) fed by a digital pulse-train of periodicity 10 us from a pulse voltage source (Figure 2.11(a)). In real-life applications, the pulse-train can be generated using a digital counter output run by a free-running clock. For the reference waveform generator, C_{SW} = 1 pF, C_O = 10 pF, and N=100 are used. Hence, for the C_{SW}/C_O = 0.1 and N = 100 and 0-to-2.5 V reference waveform, the maximum quantization error is ±51 mV, occurring at the middle of the input-output curve of nonlinear subsampling based A/D [15], and the minimum quantization error at two extreme ends of the input-output curve of the A/D is ±4 uV (Equation (2.1)). The sampling and comparison rate for the comparator is 1 Msamples/sec. The output of sample-by-sample comparison results in a bit sequence that is captured using an IEEE 1149.1 compatible architecture (Figure 2.5). Subsequently, from the captured bit sequence, the analog waveform is reconstructed offline using reference waveform information, and regression models are applied to predict the specifications from the captured test response. The center frequency and gain at center frequency are tracked within an error of ±180 Hz and ±0.1 dB. The results are summarized in Table 2.2.

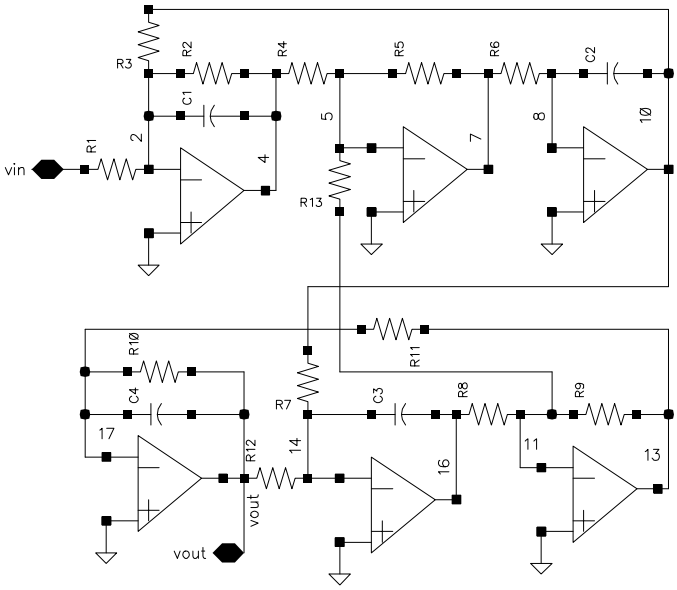


(a)

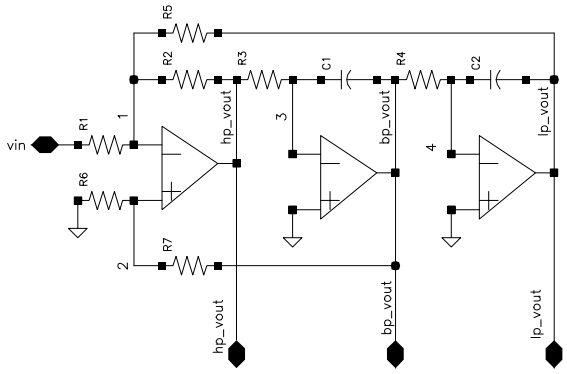


(b)

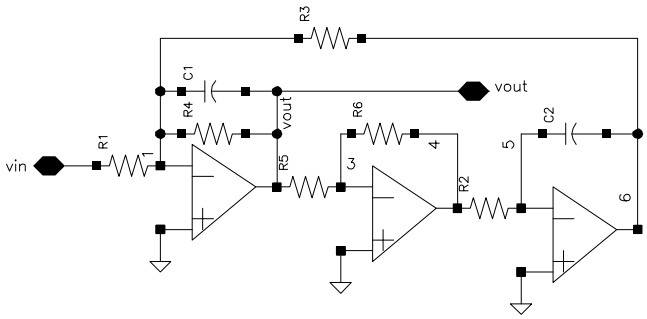
Figure 2.11. Waveforms of Tow-Thomas band-pass filter: In (a) the test response waveform (sinusoid) is compared with different voltage levels of reference waveform; the pulse-train in (a) generates the reference waveform when fed to a switched capacitor RC circuit in (b).



(a)



(b)



(c)

Figure 2.12. Schematic of (a) leapfrog filter (b) state-variable filter (c) Tow-Thomas band-pass filter.

Table 2.2. Summary of the specification prediction errors.

Circuit under test	# of critical param. perturbations	# of tones in test stimuli	# of test observation points	Max. error in spec prediction % of nominal spec. (absolute value)
Leapfrog filter	15	2	1 (vout)	LP 3dB *f*: 2.9% (± 40.6 Hz)
			2 (node 10 & vout)	LP 3dB *f*: 2.0% (± 28 Hz)
State-variable filter	11	1	1 (band-pass out)	LP 3dB *f*: 4.2% (± 45 Hz)
				BP center *f*: 5.8% (± 46.4 Hz)
				HP 3dB *f*: 3.0% (± 18.3 Hz)
			2 (low-pass & high-pass out)	LP 3dB *f*: 2.0% (± 21.4 Hz)
				BP center *f*: 2.1% (± 16.8 Hz)
				HP 3dB *f*: 1.8% (± 10.1 Hz)
2^{nd} order Tow-thomas filter (band-pass)	7	1	1 (primary o/p, using subsampling based digitization and offline waveform reconstruction)	Center *f*: < 1.8% (± 180 Hz)
				Gain at center *f*: < 0.1 dB

2.6. Limitations and Trade-offs

The primary limitations of the proposed test observation point selection approach lies in the fact that the initial analysis (prior to final test point selection using test stimulus optimization) for determining probable test observation points uses frequency response information at different circuit nodes. Although for analog filter circuits this method is effective in increasing the specification prediction accuracy (Section 2.5), this approach does not aid in determining probable test points for highly nonlinear circuits, e.g. PLLs. For such

nonlinear circuits, multitone test stimulus optimization will be prolonged, as many test nodes may not be eliminated beforehand using an initial frequency response analysis. On the other hand, for analog test response capture using the vernier digitization scheme, effective test response capture time is increased because of the serialization of databits for capturing via a digital scan architecture. Hence, the test time is traded off in this digitization approach in favor of eliminating high-resolution and fast A/D, thus, reducing on-chip test area overhead.

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CHAPTER 3

SPECIFICATION TESTING OF WIRELESS RECEIVER FRONT-ENDS

In the previous chapter, an alternate testing technique using efficient test response waveform observation was described. The concept of the alternate testing technique is further extended to RF receiver front-ends using spectral measurements.

3.1. Specification Testing Problems for RF Front-ends

The key problems with testing RF receiver subsystems are the following:

- The cost of testing complex RF test specifications is high, and at high frequencies there is a further increase in the costs.
- Any viable automated test generation algorithm requires repeated simulation of the device under test. The cost of such repeated simulations is prohibitive for complex RF subsystems [1].

In this chapter, a new test generation approach for RF subsystems is presented that handles the issue of high test cost of RF subsystems in the following manner:

Alternate tests ([2], [3]) are used to test the RF subsystem. In the alternate testing approach, the test specifications of the circuit-under-test are not measured directly using conventional methods (such as circuitry and stimulus to measure common-mode-rejection-ratio (CMRR), for example). Instead, a specially crafted stimulus is applied to the circuit-

under-test, and the (conventional) test specification values are computed (predicted) from the observed test response. In general, all the test specifications can be computed from the response to a single applied test stimulus. In the presented work, a single alternate test consisting of an optimized multitone AC stimulus is used. This is in contrast to the past alternate test method, which used a test stimulus [4] unsuitable for RF testing.

All the RF subsystem test specifications are computed (predicted) from the response of the RF subsystem to the multitone AC stimulus. Hence, significant test time savings are obtained. At the same time, the quality of the alternate test is high form the viewpoint of fault coverage and yield coverage.

Note that in the alternate test, the test limits can be set [2] so that a small number of marginal circuits are subjected to the conventional specification tests. In this way there is no loss in fault and yield coverage resulting from the use of the alternate test itself. The issue of the high simulation cost of RF subsystems is addressed in the following manner:

- Behavioral models ([1], [5]) are used to simulate the RF subsystem. By perturbing the behavioral model parameters, the correlation between the perturbation in the test response resulting from an applied multitone stimulus and the corresponding perturbation in the test specifications can be monitored. In this way, it is possible to determine how accurately all the test specifications are computed (predicted) from the observed test response.
- After the tests are generated, the quality of the tests can be determined by studying how the test specifications of an RF subsystem as well as its response to the computed multitone AC test stimulus are affected in the presence of process/circuit parameter variations. From this, the quality of the computed test (discussed later) can be

determined. This is a one-time simulation study as opposed to the many simulations needed during test generation.

As will be shown in a case study, a common test specification such as the system gain and the third order intercept (IIP3) specification for receive channel of a wireless transceiver, can be predicted using the proposed test methodology with an error below 1 dB.

3.2. Basic Concepts

The proposed approach uses the alternate testing concept first proposed by [2] for analog circuits. It shows that the variation of any process or circuit parameter, such as width of a FET, value of a resistor, etc., in the process or circuit parameter space $\boldsymbol{P}$ affects the circuit specification $\boldsymbol{S}$ by a corresponding sensitivity factor. Let $\boldsymbol{M}$ be the space of measurements (amplitudes values of subsystem output spectrum, for example) made on the circuit-under-test. The variation in the parameters also affects the measurement data in the measurement space $\boldsymbol{M}$ of the circuit by a corresponding sensitivity factor. Figure 3.1 illustrates the effect of varying one such parameter in $\boldsymbol{P}$ on the specification $\boldsymbol{S}$ and the corresponding variation of a particular measurement data in $\boldsymbol{M}$. Given the parameter space $\boldsymbol{P}$, for any point in $\boldsymbol{P}$, a mapping function (nonlinear) onto the specification space $\boldsymbol{S}$, $f:\boldsymbol{P}\rightarrow\boldsymbol{S}$, can be computed. Similarly, for the same point, another mapping function (nonlinear) onto the measurement space in $\boldsymbol{M}$, $f:\boldsymbol{P}\rightarrow\boldsymbol{M}$, can be computed. Therefore, for a region of acceptance in the circuit specification space, there exists a corresponding allowable "acceptable" region of variation of parameters in the parameter space. This in turn defines a region of acceptance of the measurement data in the space $\boldsymbol{M}$. A circuit can be declared faulty if the measurement data lies outside the acceptance region in $\boldsymbol{M}$.

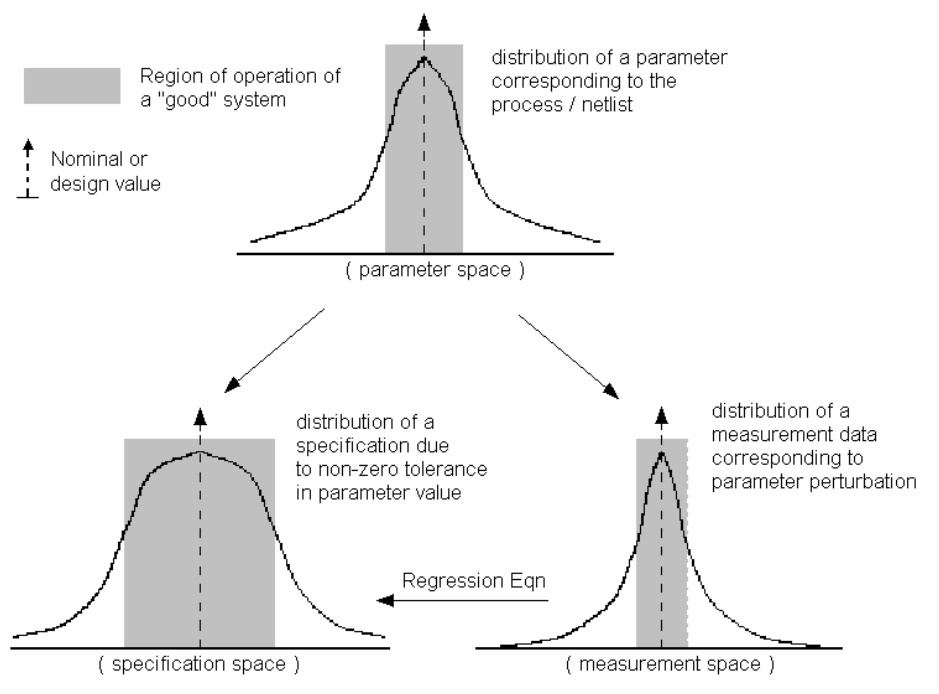


Figure 3.1. Variation in process or circuit parameter and its effect on specification and measurement.

Alternatively, as shown in [2] and [3], a mapping function $f: \boldsymbol{M} \rightarrow \boldsymbol{S}$ can be constructed for the circuit specifications $\boldsymbol{S}$ from all the measurements in the measurement space $\boldsymbol{M}$ using nonlinear statistical multivariate regression. Given the existence of the regression model for $\boldsymbol{S}$, an unknown specification of a system-under-test can be predicted from the measured data. In the proposed approach, Multivariate Adaptive Regression Splines (MARS) [6] are used to construct the regression models and estimate the test specifications of the subsystem from the frequency spectrum of the test response waveforms. The objectives of the proposed test methodology are:

1. to find a simple test stimulus (i.e. the multitone sinusoid),
2. to predict circuit specifications accurately from the alternate test response.

3.3. Test Architecture and Test Approach

The test architecture relies on the application of a multitone test stimulus designed to maximize the ability to predict the system-level specifications from the observed frequency spectrum of the test responses. In general, the stimulus can be generated externally using an RF source [7] (see Figure 3.2) or can be generated using the transmit RF subsystem. In this work, we assume the simpler test scenario in which an external RF source is used. If the transmit RF subsystem is used, the kinds of test tones that can be used to test the RF receive subsystem are limited to the signals that can be produced at the output of the RF transmit path. The test generator described in this work can accommodate such constraints with minor changes. Moreover, an approach similar to that for testing the RF receive subsystem described in the case study can be used to test the RF transmit path as well, thereby allowing comprehensive testing of the complete system.

An analog multiplexer is used to isolate the test stimulus in test mode from the functional input of the circuit corresponding to its normal operational mode. For example (Figure 3.2), to test the specifications (e.g. gain, IIP3 for the RF subsystem) of the RF receive channel of a wireless transceiver system, the input from the duplexer is bypassed using the multiplexer in test mode, and the test stimulus is applied from an RF signal generator. The amplitude spectrum of the test response waveform is used as the measurement space for the subsequent prediction of the specifications. For testing an RF receive channel transceiver, the measurements are made using a spectrum analyzer at the output of the down-converting mixer module (Figure 3.2).

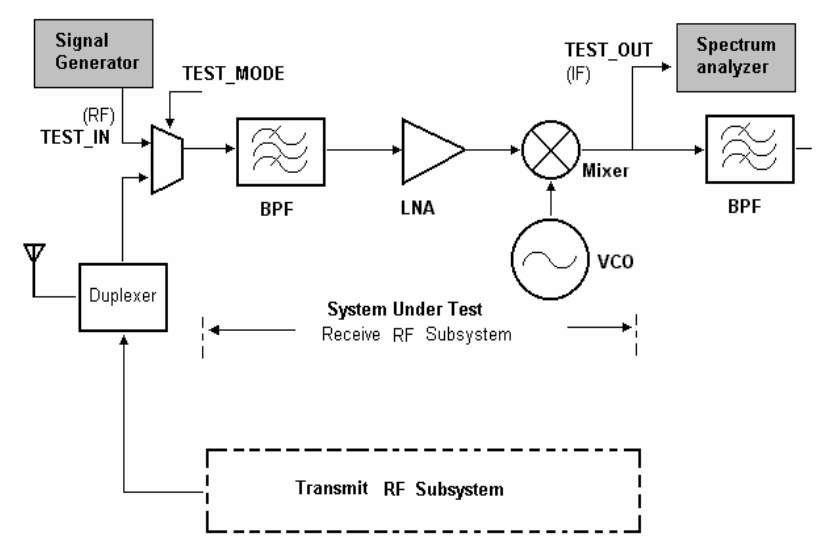


Figure 3.2. Test architecture for testing of the RF subsystem of receive channel of a transceiver.

The test stimulus consists of large-signal sinusoidal multitones (to expose the nonlinearity of the sub-modules (e.g. LNA, Mixer etc.) of the RF subsystem-under-test). In the simplest case, the test stimulus consists of two-tone 'large-signal' sinusoids, which, after being transformed through different cascaded blocks of the subsystem, exhibit the effects of linear small-signal gain as well as the nonlinear effects of harmonics and inter-modulation. A test generation algorithm using subsystem-level simulation is used to determine the different parameters (e.g. amplitudes and frequencies) of the test stimulus tones. The subsystem simulations are performed using behavioral models, as described in the following section.

3.4. System-Level Behavioral Simulation for Test Generation

An iterative search algorithm is used to determine the optimum values of the parameters of the multitone test stimulus that give the maximum specification prediction accuracy.

3.4.1. Objective of Behavioral Simulation

Behavioral-level simulation of the system-under-test is performed during the test search process for the following reasons:

First, any iterative and deterministic test generation technique (in contrast to random or pseudo-random test technique) requires repeated simulation of the system-under-test. Although the usage of transistor-level simulations for all the sub-modules yields high accuracy of simulation, the long simulation time makes the transistor-level system simulation impractical [1]. The larger the size of the process and circuit parameter space (Figure 3.1), the more of iterations of the test generation algorithm required by the search algorithm. Similarly, the higher the size of the search-variable space (e.g. the number of tones present in the test stimulus), the larger the number of simulations required for determining the optimal combination of test stimulus parameters.

Second, the primary objective of test generation is to determine the optimal set of test stimuli (which is not a circuit design goal), rather than to verify the functionality of the design. Hence, the loss of accuracy in simulation data while using behavioral models does not hinder the search algorithm as long as the statistical trend in simulation data is maintained under parameter variations. Hence, the key assumption of the proposed test generation approach is that the variations in specification data and measurement data follow the same statistical trend under behavioral parameter perturbations as they would for transistor-level parameter perturbations.

Therefore, in the proposed test generation methodology, a dual approach is taken (Figure 3.3).

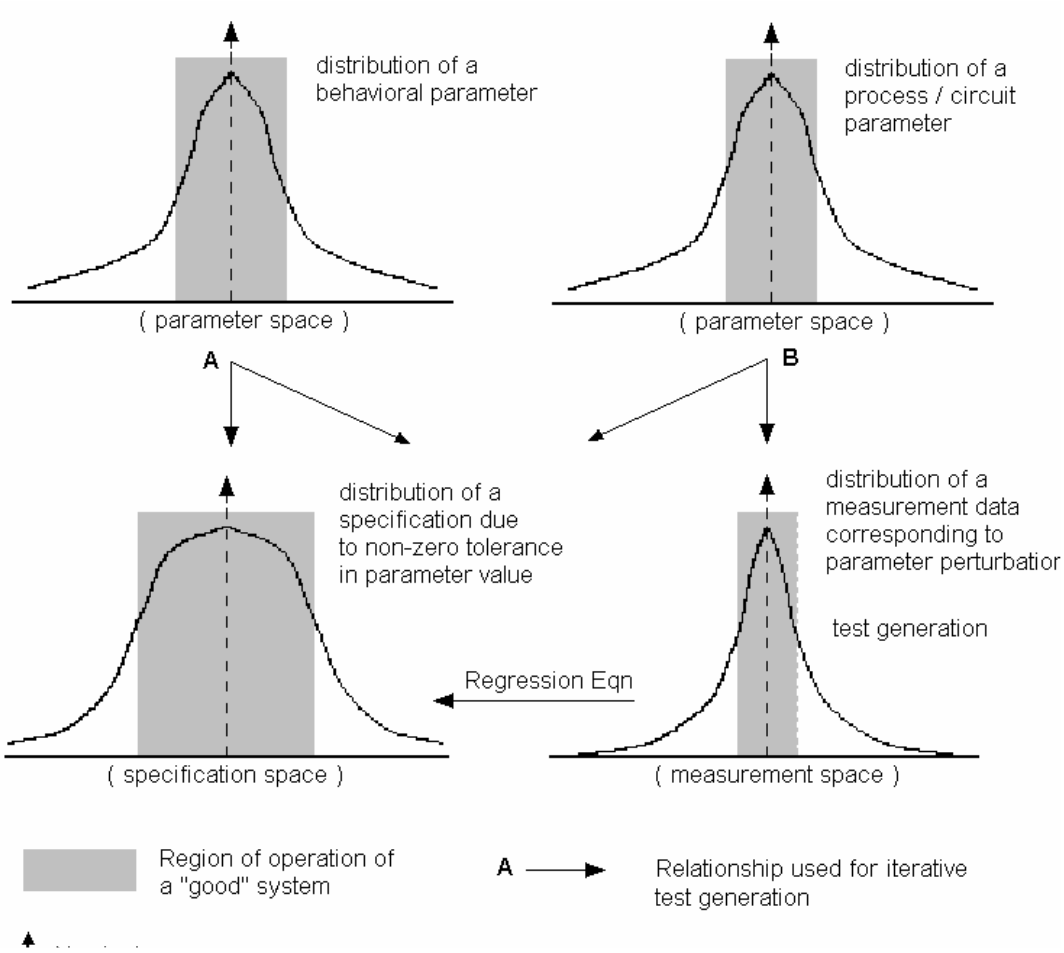


Figure 3.3. Test generation and test validation approach.

First, the test stimulus parameters are determined using system-level behavioral simulations only. Second, the resulting tests are validated against transistor-level simulations. The latter incurs a one-time transistor-level simulation cost (in contrast to repeated transistor-level simulations over different iterations of the algorithm) after the optimized test is computed by the test generation algorithm. The limitations resulting from the less accurate behavioral simulation of the test generation process are successfully overcome during test validation; the final regression models computed using transistor-level simulation data can be used for accurate prediction of the subsystem specifications.

Since the measurement space is selected to be the amplitude spectrum (i.e. amplitude vs. frequency) of the test responses observed at the output of the RF subsystem-under-test, all the simulations for test generation can be performed in the frequency domain. The behavioral models used in the test generation procedure are described next.

3.4.2. Behavioral Modeling of Sub-Modules

An RF subsystem in a super-heterodyne narrowband wireless RF transceiver architecture contains amplifiers, filters, mixers, frequency synthesizers etc. operating in a certain range of frequency (Figure 3.5). The behavioral simulation engine is developed in MATLAB. The sub-modules of the RF subsystem are modeled as follows:

Filter: For test generation purposes, the band-pass filters of the RF subsystem (e.g. band-select filter) transfer functions are realized as linear transfer functions with different gains at different frequencies. The output of the filter is given by:

$$[\ Y(f)\ ] = [\ H(f)\ ]\ .\ \mathrm{diag}(\ [\ X(f)\ ]\ ) \qquad \textbf{(3.1)}$$

where, f is the frequency of operation. The different gain values corresponding to different frequencies are characterized by the center frequency, filter-Q, and frequency roll-off. H, X, and Y are complex quantities representing amplitude and phase values together. The computation complexity for generating the mixer output spectrum is $O(N)$, where N is the number of tones present in the input.

Amplifier: The amplifiers of the RF subsystem (e.g. LNA) are realized by implementing a nonlinear transfer function of the type ([9], [10])

$$y(t) = \alpha_0 + \alpha_1\, x(t) + \alpha_2\, x^2(t) + \alpha_3\, x^3(t) \qquad \textbf{(3.2)}$$

where, α_0 = DC offset

α_1 = small signal gain

α_2, α_3 = nonlinearity coefficients

are used to realize the linear (gain) and nonlinear (harmonics and inter-modulation terms) effects of the amplifier. For inputs with sufficiently low amplitude levels, as is the case for RF subsystems, the higher-order terms (α_4, α_5 and so on) can be ignored, as they have little effect compared to the lower-order terms [1]. It is also assumed that the DC offset does not propagate across the cascade of sub-modules in narrowband RF subsystems; hence, $\alpha_0 = 0$. α_1 is characterized by the small-signal gain of the amplifier. α_3 is computed from the –1 dB compression point of the amplifier [1]. Hence, the small-signal gain and –1 dB compression point computed from the transistor-level simulation of the amplifier characterize the behavioral model of the nonlinear transfer function.

Evidently, the time domain input-vs-output characteristic, as in Equation (3.2), may not be used directly for frequency domain simulation. The output frequency spectrum (magnitude and phase) for any *x(t)* expressed as the sum of different tones can be computed as follows.

Given that Equation (3.2) is a polynomial in *x(t)* of order 3, it can be shown that, for a 3-tone input, $x(t) = V_m \cos(2\pi f_m t + \phi_m) + V_n \cos(2\pi f_n t + \phi_n) + V_p \cos(2\pi f_p t + \phi_p)$, the harmonic terms of the spectrum will be generated at:

$f =$ *0, f_i, $2f_i$ and $3f_i$* frequencies, where $i \in \{m, n, p\}$. The intermodulation product tones of the output spectrum will be generated at:

$f =$ f_i frequencies, where $i \in \{m, n, p\}$;

$f = |f_i \pm f_j|$ frequencies, where $i, j \in \{m, n, p\}$ and $(i-j)^2 > 0$; and,

$f = |\pm f_i \pm f_j \pm f_k|$ frequencies, where $i, j \in \{m, n, p\}$, and $(i-j)^2(i-k)^2 + (j-i)^2(j-k)^2 + (k-i)^2(k-j)^2 > 0$.

The corresponding amplitudes are computed using simple algebraic formulae as summarized in Table 3.1. In Table 3.1, the amplitude values V_i, etc. are complex quantities

representing magnitude and phase. For inputs having less than 3-tones, the remaining amplitude and frequencies in $\{m,n,p\}$ are set to zero and the same computation is carried out. A single-tone stimulus, for example, $V_n = V_p = 0$, will result in all the intermodulation terms to be zeroes for different f's.

Table 3.1. Amplitude vs. frequency output for a nonlinear transfer function.

	f	Output amplitudes
harmonics	0	$0.5\ \alpha_2 V_i$
	f_i	$\alpha_1 A_i (1 + 0.75\ V_i^2)$
	$2f_i$	$0.5\ \alpha_2 V_i^2$
	$3f_i$	$0.75\ \alpha_3 V_i^3$
intermodulation	f_i	$0.75\ \alpha_3 V_i^3 (-1 + {}^N\Sigma_k (V_k^2 / V_i^2))$
	$\lvert f_i \pm f_j \rvert$, $(i-j)^2 > 0$	$0.5\ \alpha_2 V_i V_j$
	$\lvert \pm f_i \pm f_j \pm f_k \rvert$, $(i-j)^2(i-k)^2 + (j-i)^2(j-k)^2 + (k-i)^2(k-j)^2 > 0$	$0.75\ \alpha_3 V_i V_j V_k$

For input having N-tones, $N > 3$, all possible distinct combinations of $\{m, n, p\}$ from N-tones are selected and the computation for the 3-tone case is carried out ${}^NC_3$ times. Hence, in general, the computation complexity is $O(N^3)$. Figure 3.4 shows a simplified flowchart for computing the output spectrum for the nonlinear transfer function, as shown in Equation (3.2). Further, for a typical nonlinear amplifier input vs. output transfer function curve, the transfer function exhibits odd symmetry, implying that α_2, α_4, α_6 etc. = 0. Hence, α_2 is assumed to be zero.

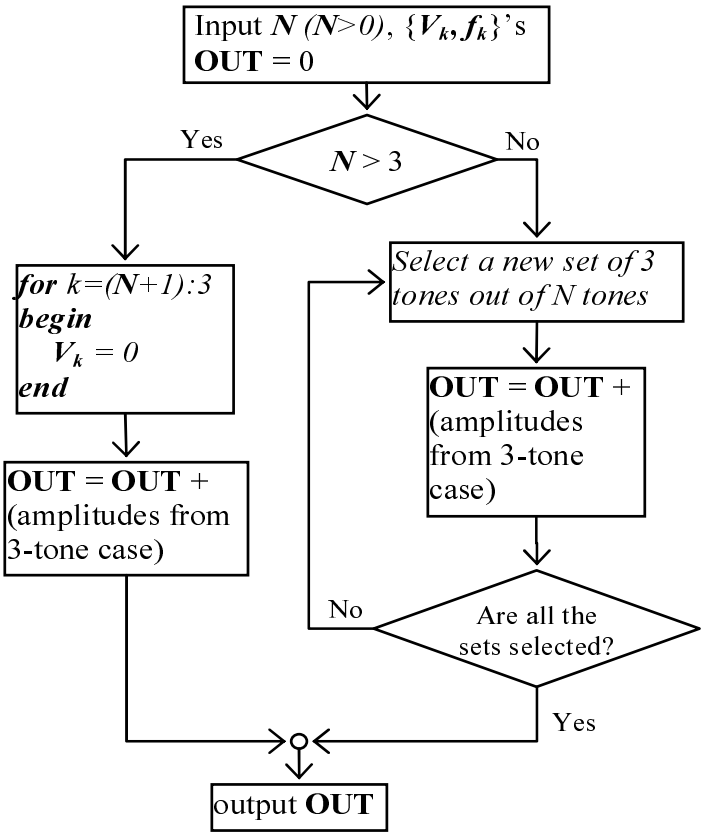


Figure 3.4. Computation of nonlinear transfer function.

Mixer: For test generation purposes, the mixer of the RF subsystem is modeled as a nonlinear transfer function followed by an ideal multiplier. The nonlinear transfer function is realized in the same manner as is done for the amplifier. The frequency mixing operation is realized by the multiplication operation.

$$y(t) = C \cdot x_1(t) \cdot x_2(t) \qquad \textbf{(3.3)}$$

The constant C is computed using the conversion gain of the mixer. Assuming a narrowband system, the conversion gain is effectively constant over the range of frequencies of interest. For $x_1(t) = V_m \cos(2\pi f_m t + \phi_m)$ and $x_2(t) = V_n \cos(2\pi f_n t + \phi_n)$, the intermodulation spectrum is generated at $f = |f_m \pm f_n|$ frequencies. Hence, the conversion gain and –1 dB

compression point with respect to the RF input and IF output characterize the behavioral model of the mixer. The computation complexity for generating the mixer output spectrum is $O(N^3)$, where N is the number of tones present at the mixer signal-input.

Oscillator: The behavioral model of the frequency synthesizer or oscillator is realized as a set of amplitude values [X*(f)*] corresponding to different frequencies. The peak amplitude value corresponds to the local oscillator frequency; the amplitudes adjacent to the frequencies fall off according to the values calculated from the phase-noise of local oscillators.

The current behavioral models used for representing the nonlinear system are simple and approximate. However, this does not significantly affect the quality of the tests derived (see Results in Section 3.6). This is because in general, the above approximations *preserve the relative "goodness"* of one test stimulus choice versus another. Hence, the test choices made with the above behavioral models are quite close to those that would have been made if accurate simulation had been used (the latter would be difficult in practice because of the large simulation times involved). The accuracy of such behavioral models is called into question only when the test generation algorithm is close to convergence. Hence, the quality of the test results (Section 3.6) is quite close to the optimal. With more accurate behavioral models, more accurate test stimulus generation can be performed.

Figure 3.5 shows, as an example of RF system-under-test, the behavioral model of the receive channel used for simulation of a narrow-band RF subsystem and computation of gain and IIP3 specifications for the same.

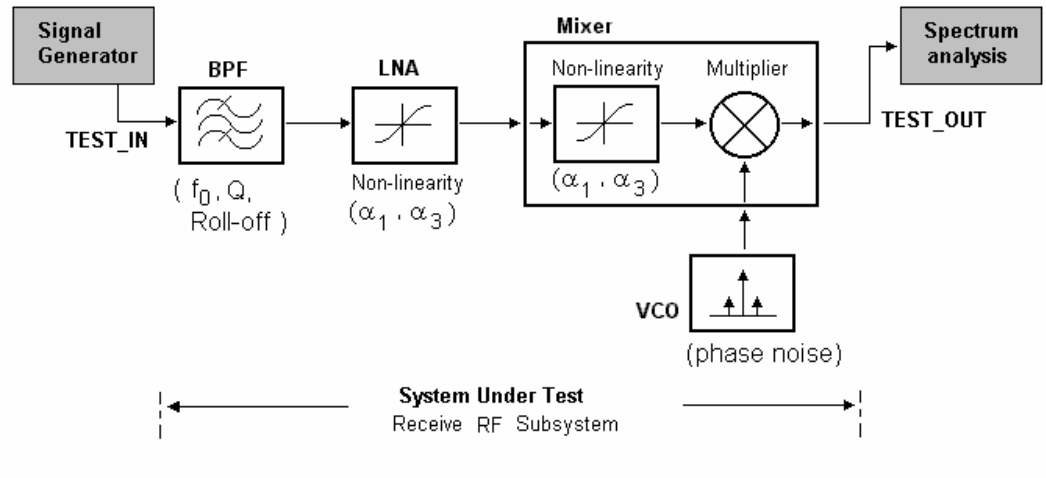
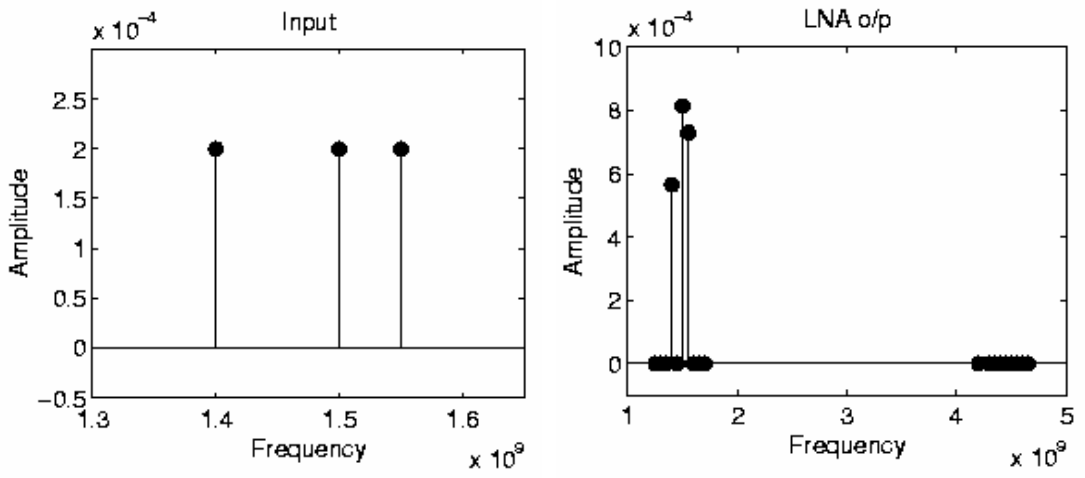


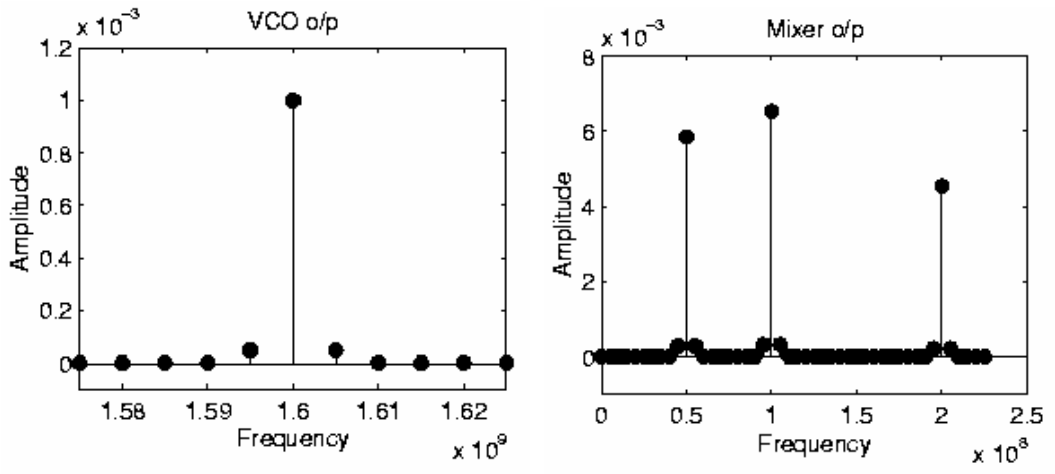
Figure 3.5. Behavioral modeling of system-under-test.

Figure 3.6 and Figure 3.7 show the amplitude vs. frequency values at the outputs of different sub-modules for the RF subsystem shown in Figure 3.5 as an example of behavioral level simulation.



(a) (b)

Figure 3.6. Example behavioral simulation: Spectrum of (a) 3 equal amplitude input tones, (b) LNA output.



(a) (b)

Figure 3.7. Example behavioral simulation: Spectrum of (a) LO and (b) Down-conversion mixer output.

3.5. Test Generation and Test Validation

An iterative greedy algorithm is used to select the parameters of the test stimulus, which is used to perform the specification test of RF subsystems. The goal of the test generation algorithm is to determine the optimal test stimulus waveform and the corresponding test response spectrum from which the specifications of the system-under-test can be predicted as accurately as possible. A multitone sinusoidal waveform *X(t)* is selected:

$$X(t) = \sum_{k}^{N} V_k \cos(2\pi f_k t + \phi_k) \qquad \textbf{(3.4)}$$

where,

V_k = amplitude for the *k*-th tone,

f_k = frequency of the *k*-th tone,

ϕ_k = phase difference of *k*-th tone with the first tone,

N = max. number of tones to be present in $X(t)$; $N \geq 2$.

The lower limit of the $\{V_k's\}$ is determined by the noise floor referred at the input of the system. The upper limit is bounded by the minimum input amplitude level that saturates any of the internal sub-modules of the RF subsystem. The lower and upper bounds of $\{f_k's\}$ are determined by the frequency range of operation for the subsystem. It may be noted that the higher the value of N, the higher the difficulty of applying the test stimulus from the signal generator. The case of $N = 2$ is the minimum value of N, for which the test stimulus undergoes the changes because of both the gain and the inter-modulation effects arising from the system nonlinearity. Furthermore, since the CUT response spectrum measured by the swept-tuned spectrum analyzers does not contain the phase information [7], for the test architecture as shown in Figure 3.2, the ϕ_k's can be removed from the test optimization variable space. Hence, in the algorithm $\phi_k = 0$, $\forall\ k$, is assumed. However, when using FFT spectrum analyzers, ϕ_k's can be included into the test optimization space to optimize the relative phase differences among the test tones for increased test accuracy.

The core test generation algorithm consists of an iterative greedy search operation, which attempts to compute the optimal values of [$\{V_k, f_k\}$'s] for a given N, such that the error in the system specification prediction is minimum.

3.5.1. Test Generation Algorithm

The proposed test generation algorithm is a variant of the gradient search [11] algorithm, which is described next.

BEGIN

// algorithm parameters:

P = nominal value of the behavioral parameters

$\mathbf{P_M}$ = Perturbation vectors in **P** for modeling regression equation

$\mathbf{S_M}$ = Specification values of the system corresponding to $\mathbf{P_M}$

$\mathbf{P_E}$ = Perturbation vectors in **P** for evaluating regression equation

$\mathbf{S_E}$ = Specification values of the system corresponding to $\mathbf{P_E}$

$Cost_2 = 0$

Input *N* of Equation (3.4)

do begin

initialize [{V_k, f_k}'s] of Equation (3.4) with some starting values within the search space

$\mathbf{OUT_M}$ = test response output spectrum for $\mathbf{P_M}$

Create regression model representing f:$\mathbf{OUT_M} \rightarrow \mathbf{S_M}$

$\mathbf{OUT_E}$ = test response spectrum for $\mathbf{P_E}$

$\mathbf{S_E'}$= evaluate f:$\mathbf{OUT_E}$ // i.e. predict specifications using regression models

Compute differences between ($\mathbf{S_E}$ and $\mathbf{S_E'}$) //i.e. error in spec. prediction

$\mathbf{Cost_2}$ = max of errors normalized w.r.t. nominal specs.

if ($\mathbf{Cost_1} > \mathbf{Cost_2}$) **then**

Perturb the current optimization point [{V_k, f_k}'s]

Compute the direction of –ve max gradient for $\mathbf{Cost_1}$ in [{V_k, f_k}'s] space

Select new [{V_k, f_k}'s] along the –ve max gradient

else

Select new [{V_k, f_k}'s] along the previously computed –ve max gradient

endif

$Cost_2 = Cost_1$

while (gradient for $\mathbf{Cost_1}$ is zero); // i.e. local minimum

END

The nonlinear regression equations in the algorithm are computed using the multivariate regression (MARS) computation engine, which attempts to map the variations in the measurement variables (amplitude spectrum of the CUT) onto the variations in the specifications of the CUT.

Figure 3.8 shows an example of cost minimization during the test generation from the behavioral simulation using two tones. The specification prediction error is used as the cost to be minimized. The test generation searches for the optimal stimulus in a three-dimensional amplitude and frequency space. In this example, the frequency of the first tone was taken as the fundamental frequency of the system, i.e. 1500 MHz. The *y* and *z* axes represent the amplitudes of two tones; the *x* axis represents the frequency of the second tone. The search algorithm is started using an initial guess (1.4 GHz, 1.3 mV, 1.1 mV). As the algorithms proceeds, it searches for the minimum cost and finally reaches a local minimum at (1.36 GHz, 1.2 mV, 1 mV), as shown in Figure 3.8. Hence, the final optimal stimulus consists of two tones at 1.36 GHz and 1.50 GHz, of amplitudes 1 mV and 1.2 mV, respectively.

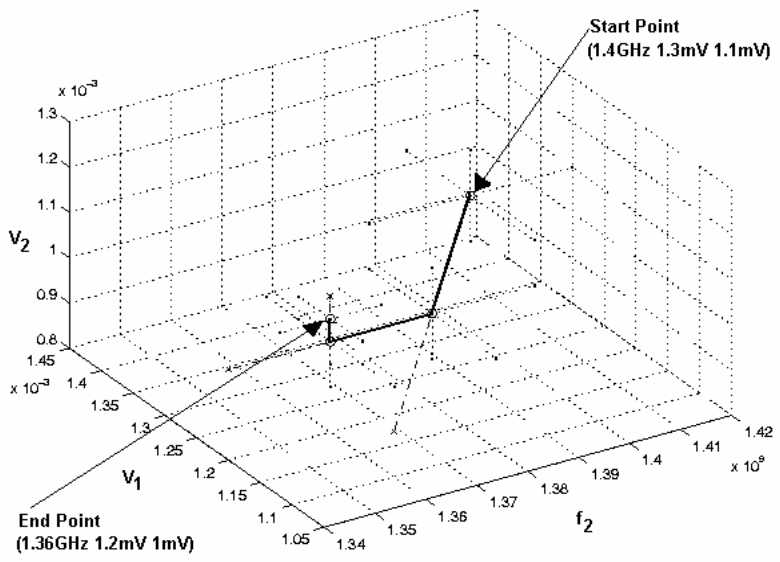


Figure 3.8. Example of prediction accuracy minimization of the test generation algorithm.

3.5.2. Test Validation Using Transistor Level Simulations

The test stimulus generated by the algorithm is validated against the transistor-level parameter perturbations as follows.

Because of process variations, the circuit components and the process parameters have non-zero tolerance values, which in effect may cause the system to fail with respect to some of its specifications. For test quality validation, the circuit (LNA, Mixer etc) component values (e.g. area of the transistors, values of R, L and C's in the modules) are perturbed and system specifications are computed for each such perturbation. In addition, the output spectrum is recorded for these multi-parameter perturbations. Although in real manufacturing process, these parameters may vary in a correlated way, random multi-parameter perturbations are used in this validation approach. The random multi-parameter perturbations of the circuit and process parameters represent the maximum degrees of freedom in which the system can fail (since, each parameter can vary independently of the other) and hence represent the worst case for test quality validation. The mapping $f:\boldsymbol{P}\rightarrow\boldsymbol{M}$ (see section 3.2) is constructed by building a regression model between the spectral components of the observed response and the specification of the system-under-test. For validation, the same function $f:\boldsymbol{P}\rightarrow\boldsymbol{M}$, computed as discussed above, is used to predict the specifications of the system-under-test from the observed response. The predicted values are compared with the corresponding specification values. If there exists a high degree of correlation between the subsystem test specifications and the response corresponding to the applied multitone test, there is little or no deviation between the predicted specification values and the specification values computed from simulation. Large deviations between the predicted and the simulated specification values would imply that the selected stimulus and the regression model have poor fitness for the RF subsystem-under-test.

In case of a high degree of fitness, the regression model and the selected test stimulus can be used together for the simultaneous testing of multiple specifications during the system-level testing of RF subsystems of a wireless receiver in a real manufacturing process. In addition, a high degree of fitness of the stimulus and regression models would validate the approach of generating a test stimulus for testing system specifications using behavioral simulations. In the next section, using the proposed methodology, it is shown that it is possible to track the specifications of the RF subsystem with high accuracy.

3.6. Experimental Results

In this section, a case study is shown using the receive channel of a transceiver as the system-under-test, on which the proposed test generation and test validation method have been applied (Figure 3.9).

The circuit component (R, L, C) values and sizes of the transistors of different sub-modules are varied to form the parameter space for the transistor-level description of the system. In this experiment, the tolerance in the parameter values is assumed to be 10% around their respective design values. System gain and system IIP3 are chosen as the specifications of interest. The nominal value of the system gain is 22 dB and system IIP3 is –12 dB for –10 dBm input level.

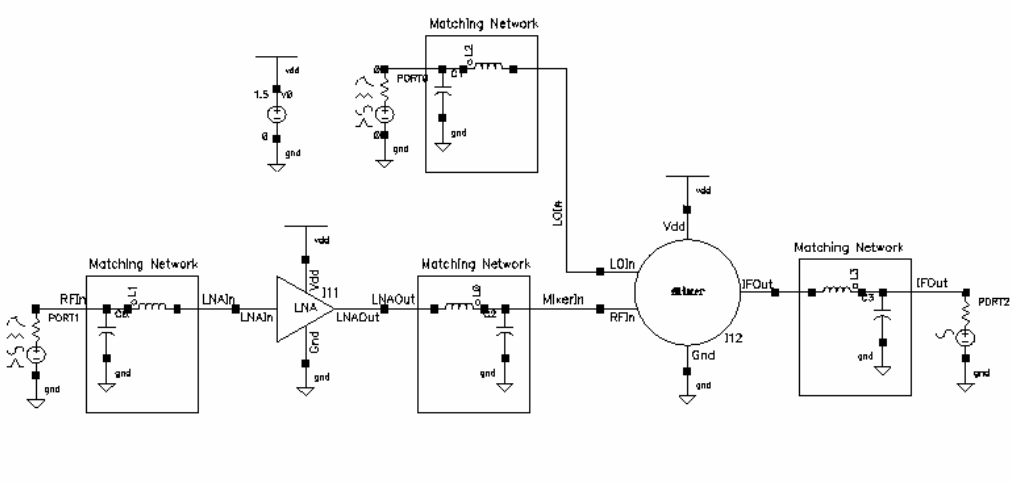


Figure 3.9. Block level diagram of the RF subsystem.

The test stimulus used had two tones, one at 1.5 GHz of 1.2 mV and the other at 1.36 GHz, the amplitude being 1.0 mV. The main features of the test stimulus obtained from the test generation algorithm are as follows:

- The stimulus consists of large-signal input tones, which try to extract the nonlinearity of the system.
- The input frequencies need not be strictly in-band tones.
- Unlike conventional specification tests, it may contain unequal amplitudes for different tones.
- The stimulus is used to compute the linear (e.g. system gain) and nonlinear (e.g. IIP3) specifications simultaneously.

The fast and greedy algorithm used in the presented work may converge at a local minimum during test optimization. However, the gradient search algorithm implementation serves the purpose of a fast optimization toolbox in the presented test generation paradigm. Other global minimum search algorithms may be used, trading off the test convergence time

for better test accuracy, without introducing any change in the methodology presented for alternate test generation.

Noise arising from the devices and parasitic elements present in the system was ignored during test generation using behavioral simulations. The test validation process uses transistor-level simulation of the system and hence inherently takes into account the noise present in the system. The test generation approach is verified by injecting parametric failures in the form of random variations of the components around their nominal values. The specifications for these circuits are predicted with the regression model. Pass/fail decisions can be made using the predicted values and the error margins, which are shown in Table 3.2. The predicted system specifications are compared with the system specification information available from transistor-level simulations. The predicted values exhibit close agreement with the specifications obtained from simulations and the majority of the predicted specification data lie in the vicinity of the straight line with slope +1, which represents the locus of "ideal" predictions.

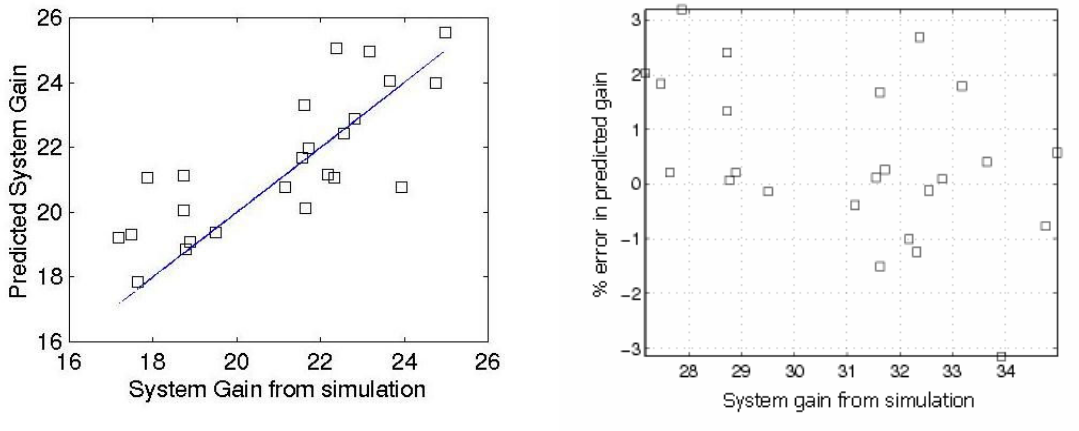
In the case study presented, every iteration during test generation for the RF subsystem using behavioral models for a two-tone test stimulus takes ~1 min, whereas the generation of the regression models from transistor-level simulations (which is equivalent to one iteration for the test generation algorithm) takes ~10 hrs. Hence, the approach presented here shows a significant reduction in test generation time by trading off simulation accuracy in the initial phase of test generation.

Figure 3.10(a) and Figure 3.11(a) show the tracking of the system gain and system IIP3 specifications. For a two-tone test, the proposed approach predicts the system-gain and system-IIP3 simultaneously, and it is possible to distinguish between faulty and fault-free circuits if the actual specification values do not lie within the prediction error margins around the upper and lower limits of their respective acceptance region. Figure 3.10(b) and Figure

3.11(b) show the percentage error in prediction with respect to the nominal values of the specifications. The results are summarized in Table 3.2.

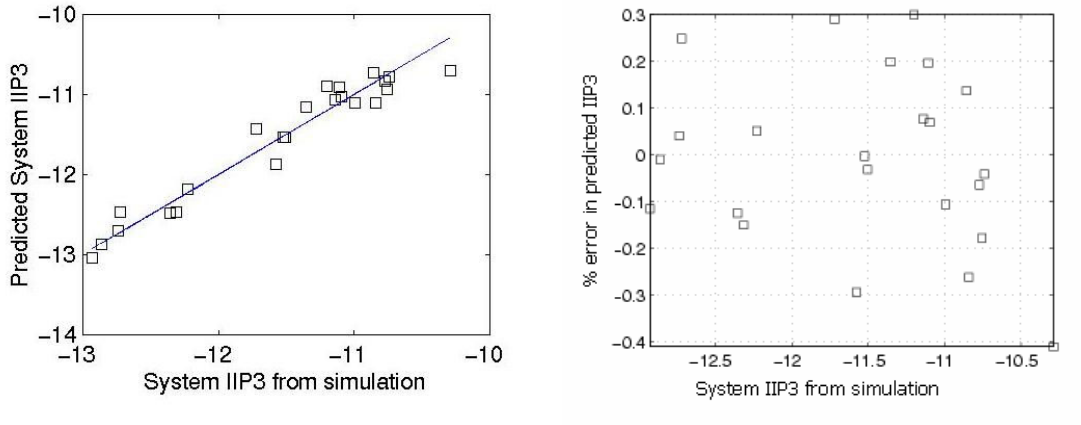
Table 3.2. Summary of the simulation results.

System Specification	Nominal value	Max. error in spec. prediction
Gain	22 dB	±3.0% (±0.7 dB)
IIP3	-12 dB	±0.4% (±0.5 dB)



(a) (b)

Figure 3.10. (a) Tracking of system gain; (b) percentage error in tracking.



(a) (b)

Figure 3.11. (a) Tracking of system IIP3; (b) percentage error in tracking.

In the presented work, the noise figure (NF), which is another important specification for the RF subsystem, was not considered. Alternate test generation for NF would require behavioral modeling of the NF-vs-frequency information from the transistor-level simulation, such that the measurement space (amplitude-vs-frequency) exhibits a statistical (deterministic) trend for predicting the NF from behavioral simulation, and the modeling incurs no significant increase in simulation time. Currently, the absence of an effective modeling approach satisfying the above constraint is prohibitive for the alternate test generation for NF.

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CHAPTER 4

SYSTEM-LEVEL SPECIFICATION TESTING OF WIRELESS RECEIVERS

In the previous chapter, alternate testing of the RF receiver front-end (consisting of LNA and down-conversion mixer) specifications has been described. The specifications of interest were gain and IIP3 of LNA and mixer. In this chapter, end-to-end specification testing of RF receiver is described, in which the frequency-domain and modulation-domain specifications of the wireless receiver are tested simultaneously.

4.1. End-to-end Production Testing of RF Receivers

In wireless communication systems, complex digital modulation schemes are used for meeting stringent spectral and SNR requirements ([1], [2], and [3]). In these systems, the overall quality of the transmission and reception are determined by various baseband and RF system specifications. Among these, the symbol error probability, commonly termed bit error rate (BER), and the error vector magnitude (EVM) are two primary specifications. These specifications determine the performance of the wireless system in terms of transmitted and received symbols corresponding to a given digital modulation scheme. Direct measurement of these specifications involves applying a test stimulus signal and capturing the test response signal at a low baseband symbol rate. In contrast, no other major specifications that determine the performance of the RF modules in wireless communications, e.g. gain, IIP3,

noise figure, receiver sensitivity, are defined in terms of transmitted and receive symbols. The latter specifications are computed using narrow-band or broadband spectral measurements corresponding to multitones, calibrated noise signals or matched terminations applied at the receiver input.

EVM is a measure of the digital modulation quality and BER is a measure of the probability of incorrect bit detection in a wireless system-under-test. The conventional symbol-oriented production test method for EVM and BER has the following implications ([4], [5], [6], and [7]):

1. For a long test response symbol sequence, measuring EVM and BER at a low baseband symbol rate incurs prolonged test time.
2. Measuring these specifications requires automated test equipment (ATE) that supports digital modulation. Hence, simple and less expensive RF signal sources may not be sufficient for EVM and BER measurement for a receiver.

In particular, the BER performance of the wireless receiver is of high importance, since a receiver often operates at an input signal power level close to the RF noise floor. For a wireless receiver, its poor BER performance can be traced back to the subsequent circuit level components of the receiver RF front-end and IF signal processing blocks [3]. From a production testing point of view, the primary objective of BER measurement for a receiver is to detect with high accuracy and repeatability whether the receiver devices-under-test (DUT) satisfy the desired BER specification for a target input signal power level. To achieve an accurate and repeatable measure of BER values in production testing, in standard testing method, a high-end RF BER tester (BERT) is required to apply and capture a sufficiently long pseudorandom bit sequence. In keeping with the decreasing manufacturing cost of wireless chipset solutions, BER testing must be performed without raising the overall testing cost for a wireless receiver.

Since the advent of wired communication, the modeling and estimation of bit error rate for communication signal paths has been of much research interest. Techniques for the accelerated BER testing of wired data-links have been reported in the literature ([8]-[11]). In contrast, with regard to efficient and low-cost production BER testing of wireless systems, little has been reported in the literature. For EVM testing, [12] and [13] showed that EVM can be estimated as a function of the intermodulation distortion effects for RF power amplifiers. However, for any end-to-end receiver, where frequency translation occurs from the RF down to the baseband, any such analysis is yet to be reported in the literature.

In this chapter, new alternate production testing techniques for receiver BER and receiver EVM have been presented. Sequences of sine tests are used for both of these tests. The test response waveforms captured in the receiver baseband are analyzed and the BER and the EVM for the receiver are predicted using the alternate test framework. In addition, using these sine tests, receiver gain, third-order-intercept (TOI), sensitivity, and noise figure can be estimated simultaneously. Alternate specification testing of gain and nonlinearity was demonstrated in [14] for RF front-ends of wireless receivers and has been described in the previous chapter. Experimental result shows that, for production testing using the proposed sine testing approach, the testing time for BER and EVM is significantly reduced. Moreover, using the proposed approach, the test instrumentation complexity is reduced.

4.2. Background of BER and EVM Testing for RF Receivers

4.2.1. BER Testing for an RF Receiver

Under the assumption that a sampled voltage value corresponding to a digital bit (part of a bit sequence received at the receiver) has a Gaussian distribution, the likelihood of error in detection, p_e, is given by:

$$p_e = 0.5 \cdot erfc\left(\sqrt{E_b / N_O}\right) \quad \textbf{(4.1)}$$

where, E_b is the energy of the received bit and the N_O is the noise power spectral density. For a system with given data-rate and noise-figure, the ratio of E_b/N_O is proportional to the SNR.

The accurate measurement of p_e, and hence the BER, requires sending a long bit sequence to the receiver and computing the ratio of the resulting number (n_{err}) of erroneous bits to the numbers of bits (N) transmitted (4.2).

$$p_e = \lim_{N \to \infty} \frac{n_{err}}{N} \quad \textbf{(4.2)}$$

From Equation (4.1), which is plotted as the p_e vs. E_b/N_O curve in Figure 4.2, it may appear that for a given noise performance when the signal power is increased arbitrarily, the p_e is decreased, resulting in an improved BER. In a practical RF receiver system, increasing the power of the RF signal does not result in a monotonic increase in BER performance of the receiver. For a given RF front-end input noise floor, increasing the RF signal power excites the nonlinear amplification characteristics of the RF front-end circuitry and the subsequent intermodulation distortion (IMD) and peak-factor (peak power to average power ratio) affect the desired in-band received signal. In other words, the SNR of the demodulated waveform in the baseband varies nonlinearly with the SNR of the RF front-end input signal.

Also, the noise figure of the RF front-end and the IF A/D quantization noise contribute to the degradation of EVM, SNR, and BER of the receiver. In effect, for a wireless receiver, the EVM and the BER performance improvement are significantly limited compared to the same found in wired communication systems.

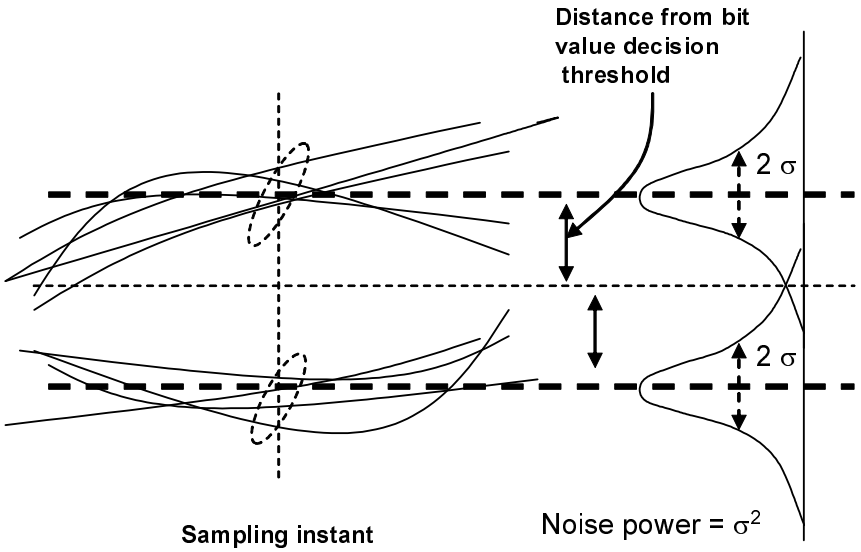

Figure 4.1. Probability of error in detecting a received bit correctly under Gaussian noise.

Depending on the presence of other different types of non-ideal behaviors of the receiver, e.g. LO phase-frequency error, I-Q gain imbalance, group-delay variation effect of the band-pass filters, the SNR of the demodulated waveform can be degraded significantly. The symbol constellation diagram provides diagnostic information regarding such non-idealities ([4], [15]). In this chapter, the term SNR is used to denote the signal-to-noise ratio of the received demodulated waveform. Low SNR is manifested by symbol scattering in the constellation diagram corresponding to the demodulated waveform in the receiver baseband.

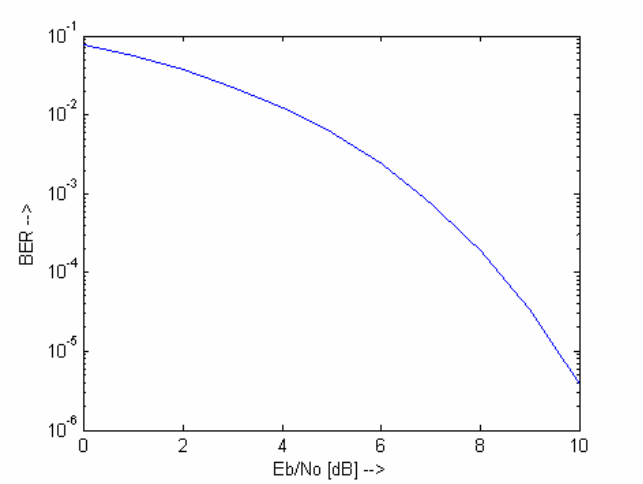

Figure 4.2. p_e **vs.** E_b/N_O **curve example.**

In addition, the values of SNR and the BER are dependent on the receiver architecture and digital modulation scheme used, e.g. QPSK and OQPSK (in CDMA system), 8PSK (in EDGE system), 0.3 GMSK (in GSM system), etc. ([16], [17]). For a specific modulation scheme, the SNR/BER performance of the receiver is also determined by the inter-symbol interference (ISI) introduced as a result of the digital pulse shaping performed by the transmitter DSP and the resulting peak-to-average power ratio of the digitally modulated signal. Pulse-shaping and digital modulation in the baseband are essential for achieving smooth baseband signal transitions from one symbol to the next and a narrow RF message bandwidth and are always used in digital radio application [16]. While a higher peak-factor degrades the SNR of the demodulated waveform at the receiver baseband, a lower ISI helps in improving the SNR, e.g. QPSK/OQPSK using Nyquist filtering for baseband pulse shaping. Hence, there exists a trade-off in terms of the RF bandwidth requirement and the modulation scheme used in different communication systems. In this paper, for demonstrating the proposed alternate test-based BER testing technique, a low, digital-IF (intermediate frequency) wireless receiver using the OQPSK modulation scheme has been

used as the test vehicle. In the next section, the basic concept of alternate testing is discussed in detail.

4.2.2. EVM Testing for an RF Receiver

Error vector magnitude is computed as

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{1}^{N} \|R - S\|^2}{\|S_{max}\|^2}} \quad \textbf{(4.3)}$$

where,

R = the received symbol in vector form (I + jQ),

S = the reference symbol in vector form (I + jQ),

S_{max} = the outermost symbol in the constellation diagram,

N = number of symbols used for EVM computation, where N is sufficiently large.

Figure 4.3 illustrates the error vector for one symbol because of the received symbol being different in magnitude and phase from the *ideal* or reference symbol. The magnitude of the error vector expressed as the percentage of the reference symbol magnitude determines the EVM value for the received symbol. For multiple symbols, EVM is determined using Equation (4.3).

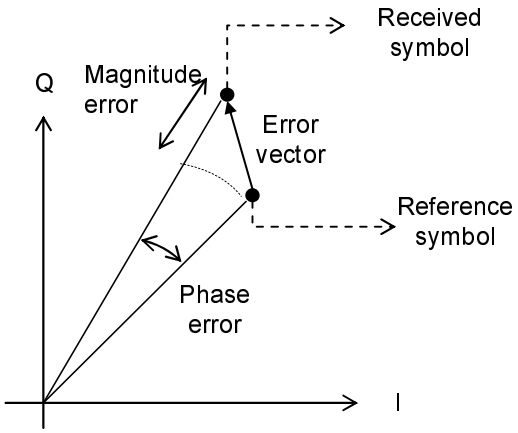

Figure 4.3. Constellation of a received symbol and its deviation from reference constellation.

In theory, for wireless systems, EVM can be measured at any RF, intermediate frequency (IF) or baseband test-point(s) where I-Q modulated signals are present. Figure 4.4, for example, shows the conventional setup for measuring EVM of an RF device whose behavior may affect the wireless data transmission performance. The EVM measurement setup for this device consists of an RF signal source supporting digital modulation and an internal down-conversion receiver for digital demodulation and symbol reception. The EVM computation block performs the required digital signal processing and computes the EVM value. Digital signal processing involves:

1. Capturing the signal samples comprising the test frame of symbols in the built-in receiver of the ATE. If there are N symbols in the test frame, and m samples per symbol, ideally $m*N$ samples need to be captured. If the baseband sampling clock rate is given by f_{CLK}, the minimum test response capture time is given by,

   $$T = m \,.\, N / f_{CLK} \qquad \textbf{(4.4)}$$

2. Sampling the received symbols at the optimal sampling point (out of m possible sampling points within a symbol) by analyzing the eye diagram for the maximum eye opening.
3. Normalizing the received symbols, so that symbol values (volts) are translated into I and Q symbol values of the constellation diagram.
4. Compensating for the constellation rotation because of phase mismatch between receiver and transmitter carrier. This rotational effect of the constellation is constant (outside the limits of phase-noise effect ([18], [19]) across the symbols of the received frame.
5. Compensating for the constellation rotation because of the frequency drift of the receiver. This rotational effect accumulates progressively and the subsequent symbols start moving away from the respective reference symbols following a circle. This is compensated by

locking the receiver modulation carrier with the transmitter carrier and/or using an adaptive digital filter in the baseband ([4], [5], [7]).

6. Computing the effective received symbol values using steps 1-5 and computing the magnitude of the EVM.

Since EVM is expressed using symbol errors computed at the symbol rate, it provides a common metric useful for comparison of performance degradation caused by different sub-modules in different stages of the receiver/transmitter and the source of error (gain imbalance, phase imbalance, phase noise, etc) ([18], [7]). Hence, for cascaded devices, EVM measurement performed on the output(s) of intermediate modules and final output provides useful diagnostic information indicating the amount of signal quality degradation and its sources.

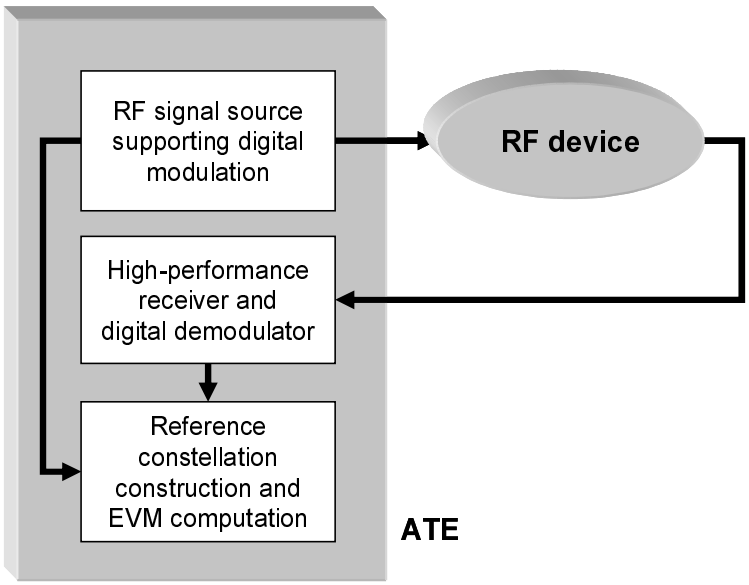

Figure 4.4. Conventional setup for measuring EVM of an RF (no baseband or IF I/O) device.

Although EVM is a useful specification for system performance diagnosis, in a highly integrated wireless system, test-point insertion for EVM measurement may not be always

possible. Second, the simplicity of the EVM specification, as expressed in Equation (4.3), translates into long test times and complex test instrumentation setup in the production ATE. For the EVM testing of a transmitter, the ATE uses a built-in high-performance receiver, whereas for the EVM testing of a receiver, the ATE uses a built-in high-performance transmitter supporting the digital modulation scheme of interest. Similarly, for RF devices having no baseband I/O, the ATE uses both the transmit and the receive hardware supporting the digital modulation/demodulation scheme of interest. In practice, EVM testing is commonly performed for the entire transmitter or receiver of a wireless transceiver, or is performed for highly nonlinear devices, such as PAs ([12], [13]). In the proposed work, a wireless receiver is used as the test vehicle for testing EVM using a multitone test stimulus sequence. The value of EVM is predicted from the baseband test response waveforms using the alternate test framework [20].

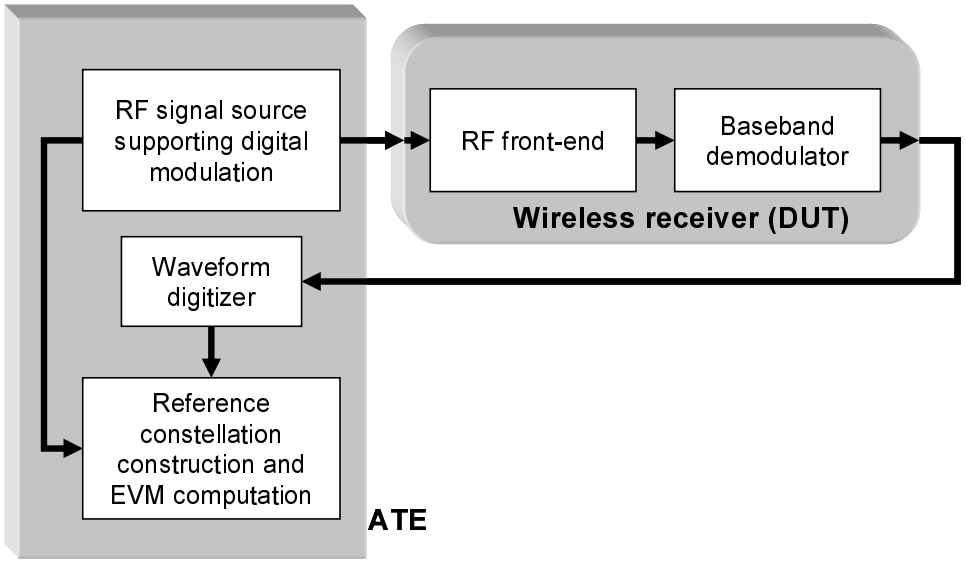

Figure 4.5. Conventional setup for measuring EVM of a wireless down-conversion receiver.

4.3. Alternate Tests for BER and EVM Testing

In the literature, the concept of alternate testing was introduced by [20]. It showed that the variation of any circuit parameter alters the circuit specifications (***S***) by its corresponding sensitivity factor, and the variations in circuit parameters also affect the measurement data in the measurement space (***M***) of the circuit by a corresponding sensitivity factor. In the proposed production testing approach, the measurement space consists of the test response waveforms corresponding to the sinusoids applied from RF signal source.

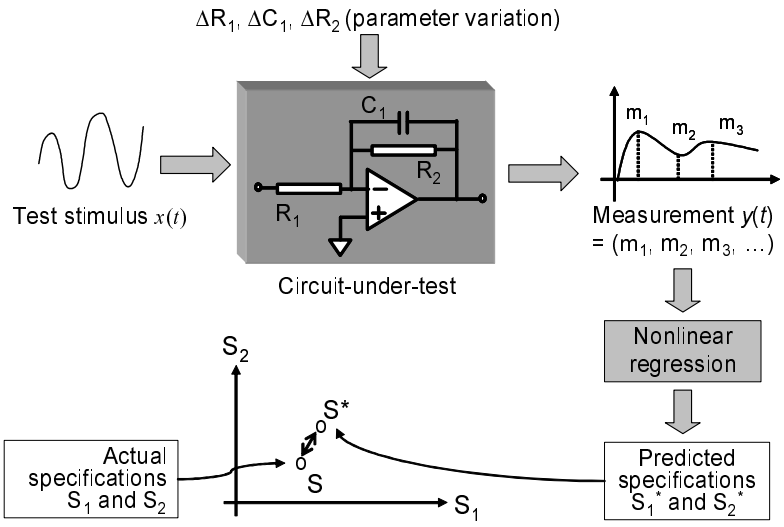

Figure 4.6. Alternate test framework.

In [20] and [21], it has been shown that for a region of acceptance (i.e. for a 'good' circuit) of the circuit specification values ***S***, there exists a corresponding allowable range of variation in all the circuit parameters ***P***, and this region of acceptance in ***P***, in turn, defines an acceptance region in ***M***. A circuit can be declared faulty if the measurement data in the measurement space ***M*** lies outside the acceptance region. Figure 4.6 illustrates the concept of

specification prediction using test response waveform samples $\{m_1, m_2, m_3, \ldots\}$ under the variation of circuit parameters, e.g. ΔC's, ΔR's, etc.

Alternatively, as shown in [20], a mapping function $f: \boldsymbol{M} \rightarrow \boldsymbol{S}$ can be computed for the circuit specifications $\boldsymbol{S}$ from all the measurements in the measurement space $\boldsymbol{M}$ using nonlinear statistical multivariate regression. Given the existence of the regression model for $\boldsymbol{S}$, an unknown specification of a CUT can be predicted with a certain accuracy from the measured data $\boldsymbol{M}$.

4.3.1. Alternate production testing for BER

For the BER testing of a wireless receiver, one can define an acceptance limit on the SNR for production testing, if the SNR vs. BER family of curves is computed during the characterization measurements performed on the bench (Figure 4.7). However, the SNR based acceptance limit must be set for the worst case BER-SNR curve (corresponding to the device having the highest SNR for the stated BER acceptance limit value) so that all the devices with higher SNR than this limit pass the BER test and no faulty device is accepted.

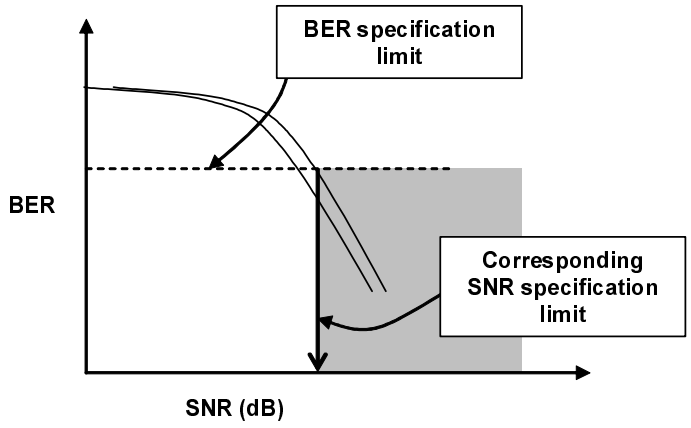

Figure 4.7. Defining the acceptance limit based on SNR measurement and BER-vs-SNR characterization curves of a particular receiver design.

Furthermore, for measuring BER, the highly nonlinear nature of the SNR vs. BER relationship and the very large range (in linear scale) of possible BER values, the relative accuracy of the values of predicted BER computed by the mapping $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$ suffers at low BER values. Hence, in the proposed production testing methodology for BER, a slightly different approach is taken.

- Two different SNR limits are used in production test: one for classifying a device as 'good' and the other for rejecting a DUT as 'bad' based on the measured SNR value for the DUT. The test limits on SNR are based on the SNR-vs-BER family of curves. The proposed AC tests are used to determine if the DUT falls into the above 'good' or 'bad' categories.
- For the remaining DUTs that are neither "good' nor 'bad' as per the above criterion (DUTs that lie in between the SNR decision limits), the BER is predicted using the $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$ regression equation discussed earlier. The predicted BER value is compared with the original BER specification limit. Multivariate Adaptive Regression Splines (MARS) [22] are used in the proposed approach to predict the BER from the test response waveforms observed in the receiver baseband.

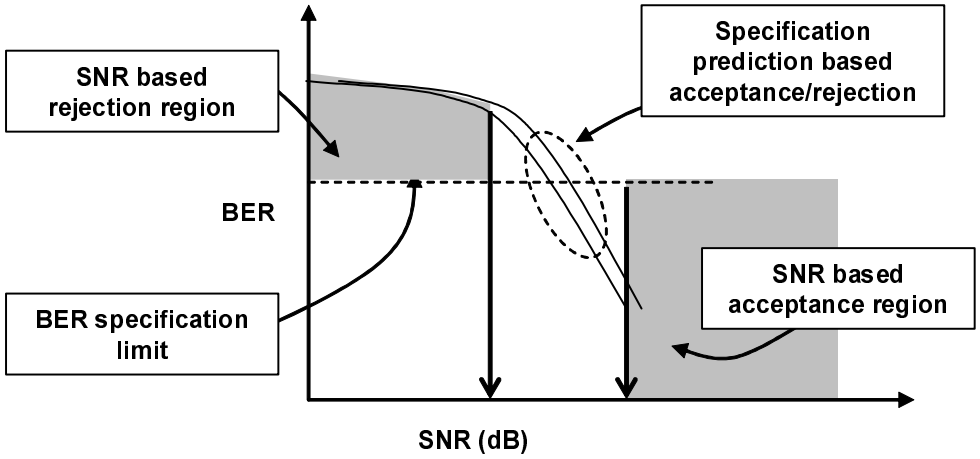

Figure 4.8. Redefining the acceptance limits for more accurate production testing.

The key advantage of the proposed production test approach is that it enables rapid BER measurement and can be easily integrated with the commonly used two-tone test framework for measuring the third-order-intercept (TOI) specification of RF circuits. The RF test instrumentation requirements are also simplified by eliminating the need for a BERT and a digital modulation-capable RF signal source.

4.3.2. Alternate production testing for EVM

In case of testing the EVM of a receiver, though the nonlinearity, noise performance and phase-frequency-gain imbalances of the individual modules affect the end-to-end EVM performance of a receiver, a closed form equation for $f: \boldsymbol{P \rightarrow M}$ is not obtainable for the nonlinear nature of interdependencies. Hence, defining acceptance limits on the frequency spectrum of the test response waveforms for separating the 'good' system instances and 'faulty' receiver instances, is by itself a complex problem. In the proposed alternate EVM testing, regression equations have been used to accurately compute (predict) the EVM specification of a receiver from a sequence of test response waveforms captured in the baseband corresponding to a sequence of two-tone test stimuli.

4.3.3. Alternate production testing for frequency-domain specifications

In addition to the BER and the EVM specification values, the frequency-domain specifications are simultaneously predicted from the baseband test response spectra corresponding to the multitone test stimulus sequence [14]. Experimental results show that using the alternate testing paradigm, gain, third-order intercept, receiver sensitivity, and noise figure specifications for the end-to-end receiver can be predicted with high accuracy without incurring additional testing time and testing hardware setup.

4.4. Test Architecture

The proposed test architecture for testing the BER specification of wireless receivers uses RF signal sources for applying a sequence of two-tone test stimuli (Figure 4.9). Two different tones are combined on the load board using a power combiner. The power-combiner is calibrated prior to test application to compensate for attenuation and isolation among the input ports. The calibration step is similar to that needed for the two-tone based IIP3 test for RF circuits. In the proposed approach, tones with the same peak power level as that of the pseudo-random message signal power in the RF domain used for performing conventional BER testing using a BERT are applied. Since the effects of receiver nonlinearities are dependent on the applied signal amplitude, the two-tone stimulus is affected in the same way by the receiver nonlinearities as the conventional BERT test stimulus using a RF modulated pseudo-random bit sequence.

The test response spectra corresponding to the two-tone test sequence are analyzed within the receiver DSP itself. Unlike the RF modulated pseudo-random pattern-based BER testing system that requires external post-processing hardware for computing the constellation diagram and determining bit-pattern matching [5], no additional hardware is required for the proposed sine-testing-based scheme. The captured spectrum at the test response observation points is used to predict the BER using the alternate testing methodology described in the previous section and a pass/fail decision is made using the predicted BER values.

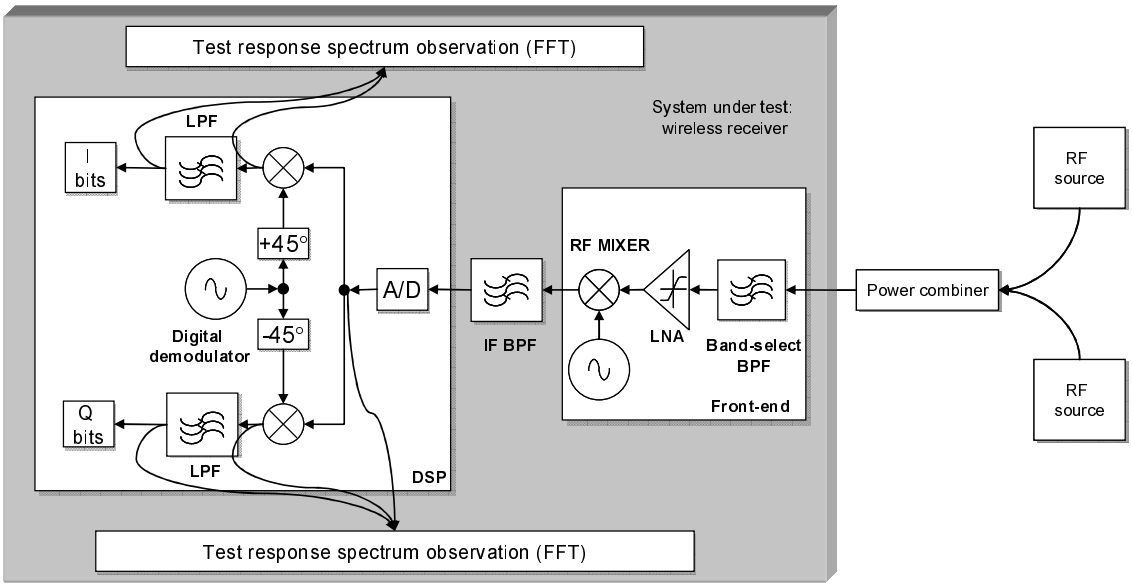

Figure 4.9. Applying two-tone test stimuli and capturing test response spectra at baseband observation points.

4.5. Test Generation

In RF test applications, unlike the low-frequency analog domain, the use of arbitrary waveform generators significantly drives up test cost. Hence, in the proposed test approach, the test stimuli are restricted to be sinusoids and at most two sine tones at a time can be applied. A two-tone stimulus is commonly used for testing the second-order and third-order intercept specifications of RF circuits. In the proposed approach, a sequence of tone pairs is used instead of only one tone pair.

The following (approximate) analysis provides the basis of applying sine tests. In this analysis, the RF front-end transfer function of a receiver is approximated using a third-order polynomial transfer function [1], given by:

$$y_{IF}(t) \approx a_1 x_{RF}(t) + a_3 x_{RF}(t)^3 \qquad \textbf{(4.5)}$$

where,

$$a_1 = SystemGain\,[V/V]$$
$$a_3 = (4/3)\cdot(SystemGain\,[V/V])/(SystemIIP_3[V])^2$$

Let the in-phase and the quadrature symbol information at radio frequency be denoted by $u_{i,RF}(t)$ and $u_{q,RF}(t)$ respectively. It can be shown that the demodulated symbol waveforms at baseband (before matched filtering) will be given by,

$$u_{i,BB}(t) = (a_1/4)\cdot\cos(\phi_{err,RF})\cdot(u_{i,RF}(t)\cos(\phi_{err,IF}) - u_{q,RF}(t)\sin(\phi_{err,IF})) + IMD_i(t) + NOISE_i(t) \quad \textbf{(4.6)}$$

and,

$$u_{q,BB}(t) = (a_1/4)\cdot\cos(\phi_{err,RF})\cdot(u_{i,RF}(t)\sin(\phi_{err,IF}) + u_{q,RF}(t)\cos(\phi_{err,IF})) + IMD_q(t) + NOISE_q(t) \quad \textbf{(4.7)}$$

where, $\phi_{err,RF}$ is the phase detection error in RF carrier recovery and $\phi_{err,IF}$ is the phase detection error for digital IF carrier recovery; and $IMD_i(t)$ and $IMD_q(t)$ are the intermodulation distortion terms, which are given by:

$$IMD_i(t) = (3a_3/256)\cdot(u_{i,RF}^2(t) + u_{q,RF}^2(t))\cdot(9\cos(\phi_{err,RF}) + \cos(3\phi_{err,RF}))\cdot (u_{i,RF}(t)\cos(\phi_{err,IF}) - u_{q,RF}(t)\sin(\phi_{err,IF})) \quad \textbf{(4.8)}$$

$$IMD_q(t) = (3a_3/256)\cdot(u_{i,RF}^2(t) + u_{q,RF}^2(t))\cdot(9\cos(\phi_{err,RF}) + \cos(3\phi_{err,RF}))\cdot (u_{i,RF}(t)\sin(\phi_{err,IF}) + u_{q,RF}(t)\cos(\phi_{err,IF})) \quad \textbf{(4.9)}$$

Hence, it is observed that, even for perfect carrier recovery (i.e. $\phi_{err,RF}$ and $\phi_{err,IF}$ are zero), the demodulated baseband signal gets distorted because of the IMD at high RF signal level (i.e. for large values of $u_{i,RF}(t)$ and $u_{q,RF}(t)$). In a linear system I and Q signals are orthogonal to each other, whereas for a nonlinear receiver transfer characteristic, the Q (I) channel signal energy falls onto the I (Q) channel and distorts the demodulated baseband signal, irrespective of the absence of any other noise sources in the system. Additionally, $NOISE_i(t)$ and $NOISE_q(t)$ are the respective noise terms for received I and Q channels, and

result from RF noise floor, noise-figure specifications of the RF front-end components and baseband A/D quantization noise.

It is readily observed that for a receiver with perfect linearity (i.e. $IMD_i(t)$ and $IMD_q(t)$ are zero) carrier recovery (i.e. $\phi_{err,RF}$ and $\phi_{err,IF}$ are zero) working in noise-less environment ($NOISE_i(t)$ and $NOISE_q(t)$ are zero) , the received I and Q symbols reduce to:

$$u_{i,BB}(t) = (a_1/4)\, u_{i,RF}(t) \quad \textbf{(4.10)}$$

$$u_{q,BB}(t) = (a_1/4)\, u_{q,RF}(t) \quad \textbf{(4.11)}$$

For this ideal condition, the RF front-end does not degrade the SNR, EVM, and BER. In this condition, these specifications are guided by the ISI occurring because of the the baseband pulse-shaping and the group-delay variation caused by the analog and RF filters in the signal path. However, for a real receiver, all the above non-idealities are present Based on the above considerations, in the proposed test methodology, the sine test stimuli are selected.

In the proposed approach, a set of two-tone stimuli is applied to the receiver under test. The sequence of two-tones is applied at $f_{LO}+f_{IF}$ (assuming upper sideband selecting receiver) and f_T, where $f_{LO}+f_{IF}$ is kept fixed and f_T is varied over the entire message bandwidth (which is decided by the baseband data-rate). In this step, the amplitudes of the applied tones are selected the same as the peak signal power values for conventional BER testing and EVM testing. The sweeping effect of the f_T captures the group-delay-variation effect caused by the filter w.r.t. the fixed $f_{LO}+f_{IF}$.

It should be noted that the larger the number of different values of f_T selected, the larger the overall specification testing time required. Hence, the selection of different values of f_T sweep is driven by the following test time reduction algorithm. The objective of procedure selecting the optimal number of test tone is to achieve the prediction error in the mapping

function (see Section 4.3) lower than a given error threshold (input to the algorithm). The inputs to the algorithm are:

1. The center frequency (f_c) and the bandwidth (BW) for the RF channel, where RF channel spreads from f_c to ($f_c + BW$).
2. Initial value of frequency Δf_T stepping for the consecutive f_T values.
3. A vector of error threshold values that corresponds to the acceptable error in prediction values (Δ_{ERR}) of the specifications.

The random search based test selection algorithm is as follows:

BEGIN

- *Input f_c, BW, Δf_T and Δ_{ERR}*
- *Measure the specifications of the receiver using conventional test set up and applying pseudo-random bit sequence for multiple receiver instances (generated by perturbing its behavioral parameters)*
- *Set $f_T = f_c$*
- ***while** (f_T is less than (f_c,+ BW)) **do***
- *set $f_T = f_T + \Delta f_T$*
- *Apply { f_T, f_{LO}+f_{IF} } two-tone (*Figure 4.9*)*
- *Capture spectral responses*
- ***endwhile***
- *Concatenate the spectral response values obtained in 6.*
- *Compute nonlinear regression models (using MARS) from the captured baseband receiver spectrum onto the specifications computed in 2.*
- *Apply the tone-pairs to a different set of receiver instances and predict the specifications using previously computed regression models*
- *Error = (predicted specification value) – (measured specification value)*
- ***if** (the maximum value of Error < Δ_{ERR}, value) **then***
- *set $\Delta f_T = 2 * \Delta f_T$ and $\Delta f_{T, final} = \Delta f_T$*
- ***goto** 3*
- ***else***
- ***exit***
- ***endif***

END

Hence, the algorithm outputs the largest frequency stepping required across the desired RF channel during alternate testing for the programmable frequency sweep parameter of one of the two RF sources. The other RF source is programmed to output a fixed tone at f_{LO}+f_{IF}.

4.6. Experimental Results

4.6.1. Simulation Results

In this section, simulation results for a 900 MHz GSM band wireless receiver are presented [23]. The results of testing for EVM and BER using the proposed alternate test methodology are compared with that of the conventional testing procedure.

A digital IF system using RF up/down-conversion is used for the simulation results. As the excessive simulation time needed for transistor-level transient simulation of the entire wireless receiver is prohibitive, the concept of using a sine test framework for BER testing is demonstrated using behavioral simulation of a 900 MHz receiver system in Matlab. For the behavioral modeling of the RF components, e.g. LNA, mixer, LO, of the receiver and the transmitter, the existing models have been used and are described in detail in [1] and [24]. The gain of the behavioral-level band-select filter is -2.7 dB. The LNA gain, IIP3 and NF are 10 dB, 4.6 dBm, and 1.6 dB, respectively. The mixer conversion gain, IIP3, and NF are 5.8 dB, 11 dBm, and 14 dB, respectively. In the baseband, data rate is 25 kbps and pulse shaping using Nyquist filtering (split over the transmitter DSP and the receiver DSP as root-raised-cosine transfer functions) is done. OQPSK digital modulation is performed at a low IF of 100 kHz. An LO of 900 MHz is used for the RF front-end. BPF at IF is realized using a digital filter approximating an analog transfer function centered at 100 kHz. Multiple instances of the receiver-under-test are generated by varying the behavioral parameters (i.e. gain, IIP3, NF, filter coefficients) by perturbing them simultaneously around their nominal values.

Case study I: BER testing: The simulation is performed frame by frame, each frame consisting of 600 data bits, generated using a pseudorandom bit sequence of period 127. Data

between I and Q channel are uncorrelated as a random shifting is applied between two bit patterns for every frame. In the baseband, a 12 bit A/D operating at the speed of 4 MSamples/s is used. The baseband simulation is performed in the time domain whereas the RF front-end is simulated in the frequency domain and an FFT/IFFT block converts the time domain data to frequency domain data and vice versa. A combination of frequency-domain and time-domain simulations is done for accelerated simulation for long bit sequences used in BER simulations. For BER computation, many frames are collected over time to generate a long bit sequence. Figure 4.10 shows the spectrum of one such data frame at 900 MHz.

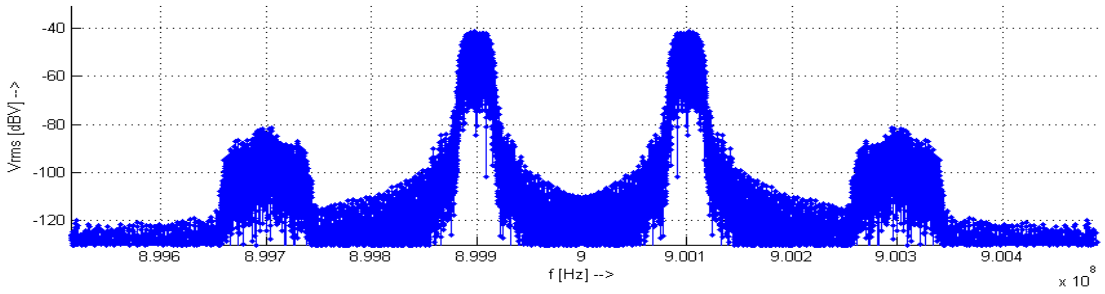

Figure 4.10. Message spectrum with RRC filtering at transmitter output (in simulation).

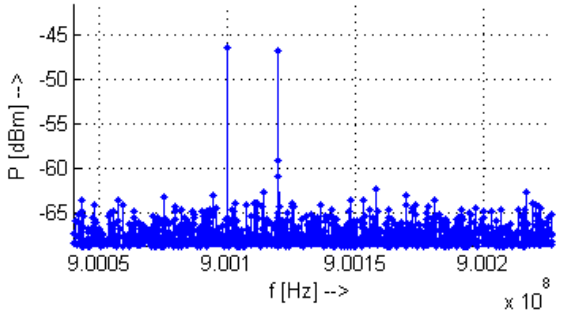

Figure 4.11. Two-tone sent at 900.1MHz (f_{LO}+f_{IF}) and 900.12MHz (f_{LO}+f_T).

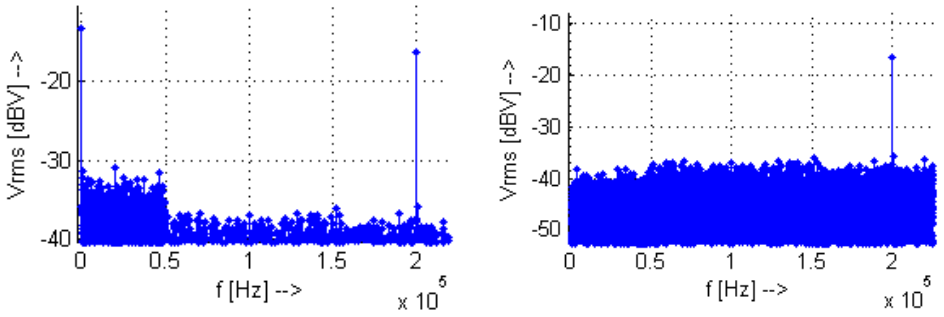

Figure 4.12. I and Q channel spectra for single-tone at 900.1 MHz.

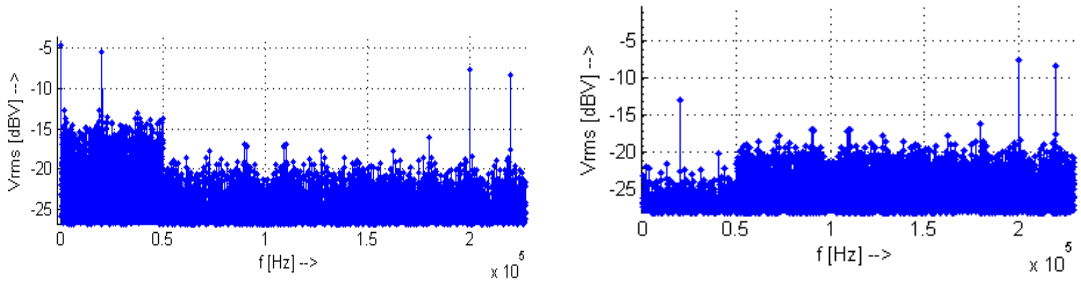

Figure 4.13. Spectrum data at baseband.

The sequence of two-tones is applied, where one tone is always at 900.1 kHz ($f_{LO}+f_{IF}$) and the other tone (f_T) is swept over the entire message band width initially at 1 kHz spacing (Δf_T) over 100 kHz, where BW is approximately equal to 50 kHz for a 25 kbps baseband datastream. The spectral power data for the signal and the IMD frequency bins and the total noise power data are collected and the regression functions f:$\boldsymbol{M \rightarrow S}$ are computed, which maps these data onto the BER using an alternate testing paradigm (Section 4.3). Then the test tone selection algorithm is applied to reduce the test time for a target BER prediction error of $1e^{-4}$, resulting in Δf_T of 4 kHz.

Figure 4.14 shows the tracking of the predicted BER ('circles') w.r.t. the simulated BER ('dots') of two different receiver instances, whose performance varies widely for the given architecture within the SNR range of 8.0dB to 9.0dB, where BER fluctuates rapidly. It is

observed, that the relative accuracy in tracking BER specification is higher for larger BER values.

In terms of time for BER testing, the simulated BER values that have been calculated by sending 10^5 data bits at 25 kbps would require approximately 4 sec of test time. This does not include the further processing time required by the BERT. On the other hand, using sine test based alternate approach the BER values are predicted by applying two-tone tests for 25, i.e. 100 kHz spectrum at 4 kHz spacing, times for 50 cycles corresponding to the baseband waveform (for computing accurate spectra using FFT in presence of noise and IMD), which would take approximately 50 ms of testing time. However, actual testing time is more than 50 ms because of the overhead of reprogramming the f_T after every 50 cycles of each tone. Allowing 200 ms (4 ms per reprogramming and settling time) for the overhead resulting from reprogramming the two-tone and settling time, the total testing time turns out to be 250 ms, giving 3.75 sec of test time savings.

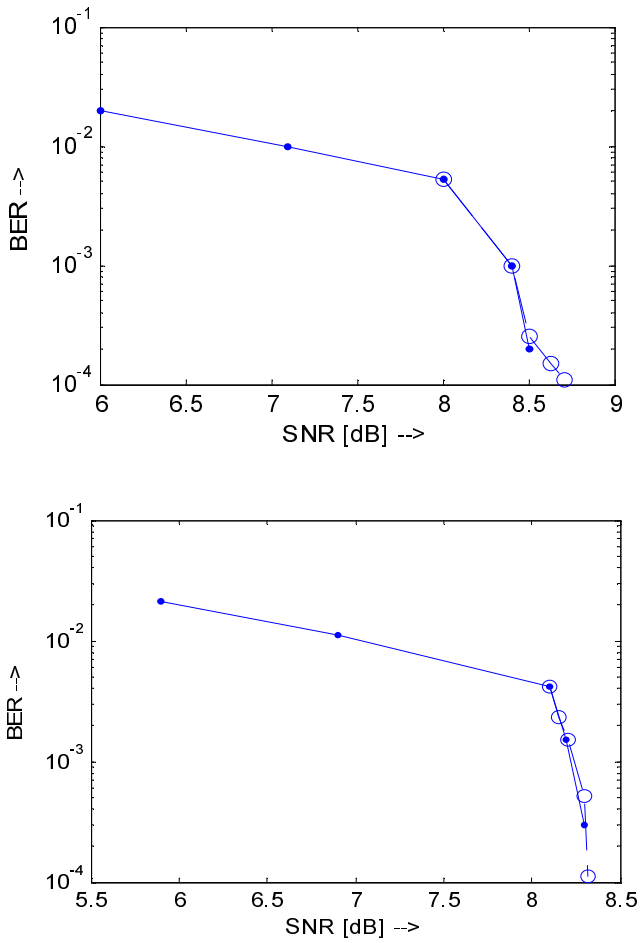

Figure 4.14. For two different devices, tracking of BER within 8.0dB to 9.0 dB SNR.

Case study II: EVM testing: The simulation is done in the time-domain using Simulink (Matlab) behavioral models for all the receiver sub-modules. For the frequency synthesizer, f_{LO} is taken to be 900 MHz with an instantaneous frequency deviation of 20 Hz. The maximum phase imbalance between the I and the Q outputs of the LO is assumed to be 5 deg and gaussian random phase is added to the nominal 90 deg phase difference. The channel-select band-pass filter center frequency is 100 kHz with a Q-factor of 5. In the baseband, a 12 bit A/D operating at the speed of 1 MSamples/sec is used. Additive noise of 0.5 LSB for the input dynamic range of ±2.5 V is assumed. The modulating frequency in the baseband is 100 kHz and the data rate is 25 kbps for each of the I and Q channels, resulting in a symbol rate

of 50k symbols/sec. The baseband DSP runs at f_{CLK} = 1 MHz. The number of samples per symbol, m = 40.

For the conventional testing procedure, a GMSK modulated pseudo-random bit sequence using BT=0.3 and symbol interval of 3 ([16], [26]) is used. The modulated bit sequence is up-converted to 900 MHz and fed into the receiver under test at -45 dBm power level, within the -1dB compression point of the LNA input. The test data frame-size for EVM measurement is taken to be 500, i.e. 1000 I and Q symbols. Figure 4.15 shows the spectrum of the transmitted frame.

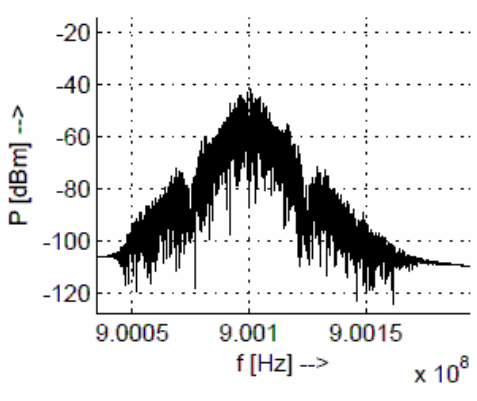

Figure 4.15. Spectrum of conventional test stimulus for EVM: GMSK modulated test data frame at 900MHz.

The received demodulated waveforms (Figure 4.16) are sampled, normalized, processed for constellation rotation and the EVM value is computed. Figure 4.17 shows the received symbol distribution in the constellation diagram. The value of EVM is computed to be 0.132 (13.2%) corresponding to the constellation diagram shown in Figure 4.17. Multiple instances of the receiver-under-test are created by varying the behavioral parameters (i.e. gain, IIP3, NF, filter coefficients) by perturbing them simultaneously around their nominal values. For each receiver instance, the corresponding EVM value is computed and used later for comparison with the results obtained using the proposed methodology.

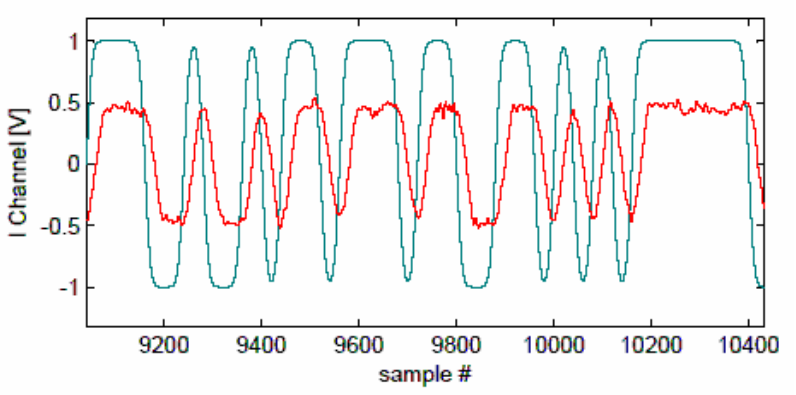

Figure 4.16. Transmitted and received I channel waveforms (smaller pk-to-pk is the received signal).

In the *alternate test framework*, multitones are applied to the RF front-end and selected as described earlier. Within the channel-bandwidth of 200 kHz, a sequence of three tone-pairs, viz. {900.1 MHz, 900.12 MHz}, {900.1 MHz, 900.14 MHz}, and {900.1 MHz, 900.16 MHz} with Vpk of 1 mV (-50 dBm) for each tone, are applied from the RF signal source for 1ms in each case. The experimental results show that for high accuracy of the regression model, the selected tone-pairs need to cover the entire bandwidth of the receiver under-test. The test response waveforms are captured at the output of the symbol samplers (Figure 4.9) at 1 MHz. The test responses are used for constructing the nonlinear regression model (see Section 4.3) that maps the test response waveform data onto the EVM specification. Given the existence of this regression model, for different receiver-under-tests (not within the training regression set, i.e. their specification values were not used for computing the regression model), the EVM are predicted. Figure 4.18 shows the tracking between the predicted values of EVM obtained using the multitone test framework and the measured values of EVM obtained using conventional EVM testing approach using digitally modulated stimulus. A high correlation value (i.e. when all scatter points are close to the straight line of slope +1 in Figure 4.18) between the predicted EVM and measured EVM shows that the

multitone test framework for EVM testing can replace the conventional EVM test framework without sacrificing test accuracy. From Figure 4.18, the maximum prediction error is ±0.03 EVM_{rms}. For the few outlier DUTs (Figure 4.18), either conventional test needs to be performed after alternate testing, or these outlier DUTs are designated as 'faulty'.

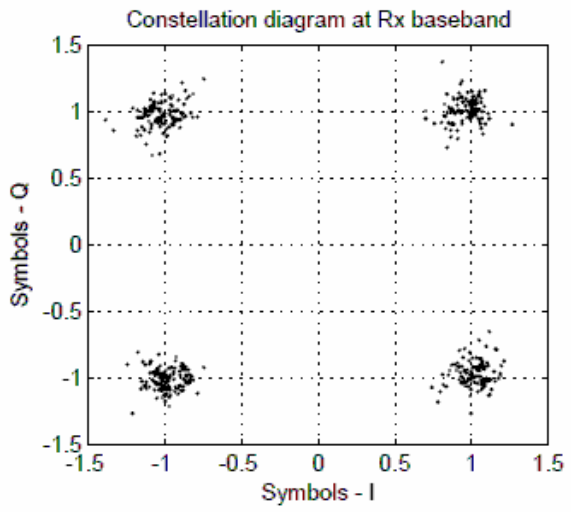

Figure 4.17. Constellation diagram for the received symbols, EVM (rms) = 0.133.

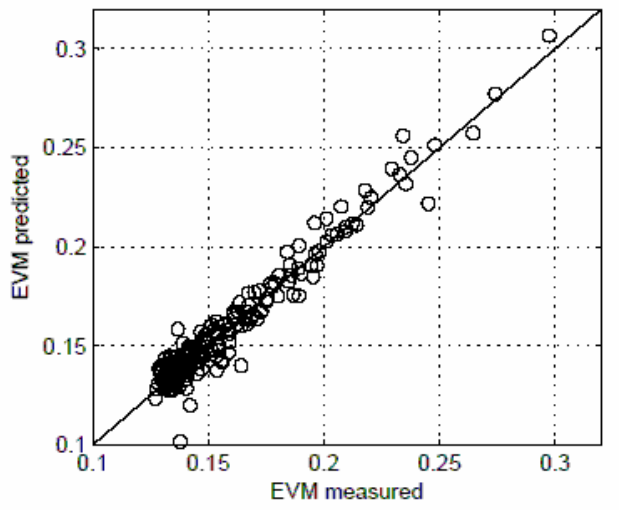

Figure 4.18. Tracking of predicted rms values (multitone stimulus) of EVM vs. measured rms values (up-converted modulated bit sequence stimulus) of EVM.

Significant test time reduction is achieved by using the multitone test framework for testing receiver EVM. In this example, assuming that the basic test time is governed by the time to apply the test stimulus and to capture the test response waveform, for conventional test approach, the total test time for a frame of 500 I-Q bits (1000 symbols) at 25 kHz is 20ms. On the other hand, in this example, the total test time for capturing three tone-pairs is 3ms.

4.6.2. Measurement Results

The proposed methodology for testing the system-level specifications is verified using a 1.575 GHz measurement setup. Figure 4.19 shows the block diagram of a measurement setup. A Matlab software interfacing a data acquisition card running at 4 MSamples/s performs all the digital signal processing functions, the test stimulus application (in Setup A), the IF test response waveform capture, test response analysis and test sequence control. OQPSK (de)modulation scheme using 100 kHz IF carrier is implemented in the baseband, where the baseband data-rate is 25 kbps.

Setup A is used for standard modulation-domain specification testing, where RF modulated data-frames are applied as test stimulus. In this experiment, data-frame size is restricted to 550 I-Q bits, where the maximum possible size is determined by the maximum number of waveform samples that can be buffered in the DAQ card at a time. Many RF modulated data-frames are applied at the RF input of the receiver-under-test and the test response waveforms are demodulated to compute the symbol constellation diagrams, eye diagrams and number of bit errors. Subsequently the EVM, magnitude-error, phase-error, modulation SNR, and BER values are computed.

Setup B is used for conventional frequency-domain specification testing to apply two-tone tests for measuring receiver gain and third-order-intercept. The proposed alternate test methodology also uses setup B to apply the tone-pair sequence as RF test stimulus.

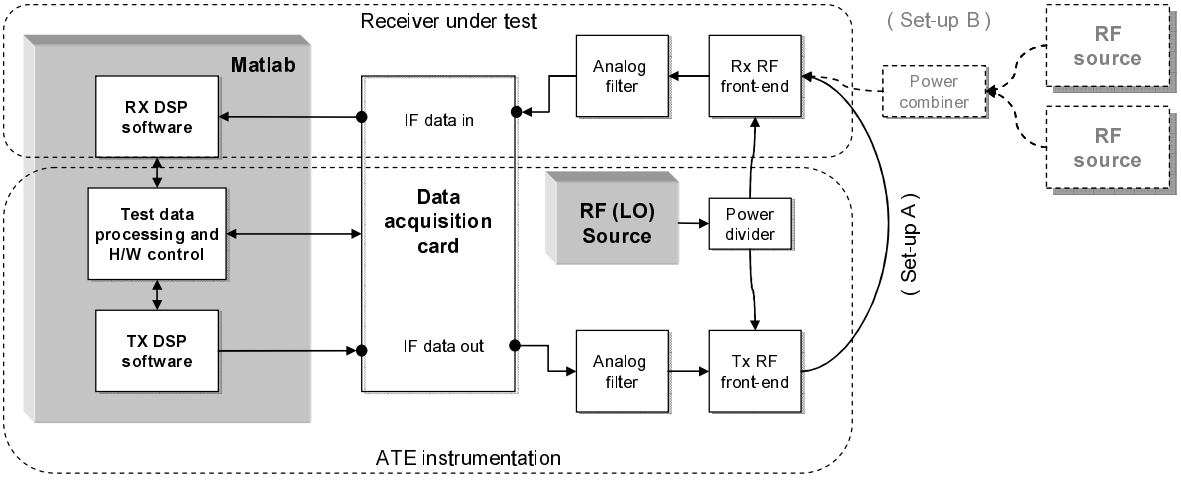

Figure 4.19. Measurement setup: Setup A used for modulation-domain specification measurement; Setup B for frequency-domain specification measurement and alternate testing of receiver.

Two case studies are presented in this sub-section, where end-to-end receiver specifications are tested at two different RF input signal power levels. In the first case, the receiver is tested at a low input signal power of -55 dBm, where intermittent bit detection errors take place to give non-zero value of BER. In the second case, the receiver is tested at a high input power level (in comparison to the IIP3 of the receiver) of -20 dBm. At this signal power-level, no bit detection errors are observed because of the much improved modulation SNR.

To generate multiple instances of the receiver, the supply voltage to the receiver front-end is varied so that the specification values of the receiver are altered over a considerable range. The proposed alternate test methodology is validated over these ranges of the specification variations. For an accurate alternate test methodology, the specification values

predicted by the alternate tests must track the corresponding specification values obtained using (prolonged) conventional tests.

Case study I:

First, for the test condition of -55 dBm RF input signal power, the receiver specifications are characterized. Figure 4.20, Figure 4.21, and Figure 4.22 show the BER, EVM, and modulation SNR specification values of many receiver instances that are generated by varying the supply voltage of the receiver front-end. The supply voltage variation has been restricted down to 2.6V. Below this supply voltage, the IF carrier recovery, the waveform demodulation, and the symbol sampling become inoperative due to poor SNR, and subsequently the receiver DSP logic drops the entire data-frames. In Figure 4.23 and Figure 4.24, the variation of the BER and EVM values w.r.t. the modulation SNR values are shown. In Figure 4.25 and Figure 4.26, two data-frame constellations consisting of 550 symbols are shown for two different modulation SNR values. EVM and BER values are measured using 200 such data frames (110k symbols) incurring prolonged test time (~45 minutes in real time that include DAQ card control and data processing overhead) for each test.

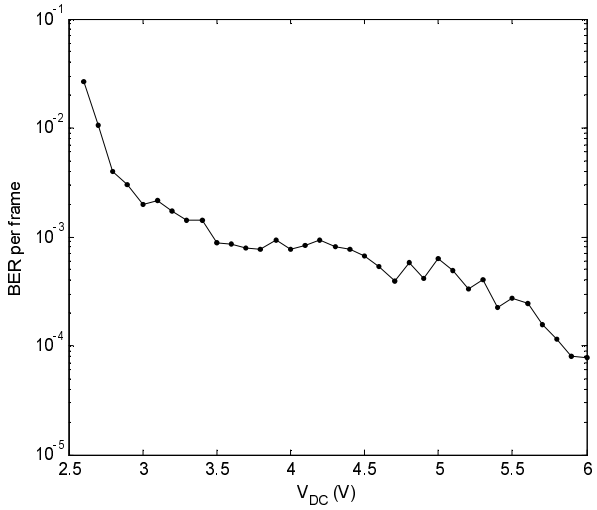

Figure 4.20. Receiver specification variation: BER.

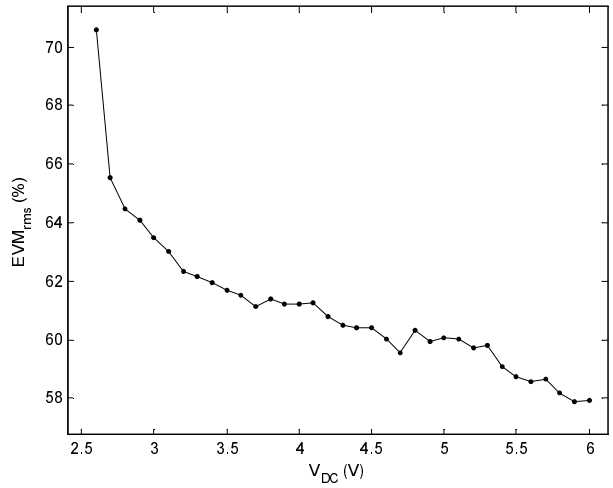

Figure 4.21. Receiver specification variation: EVM.

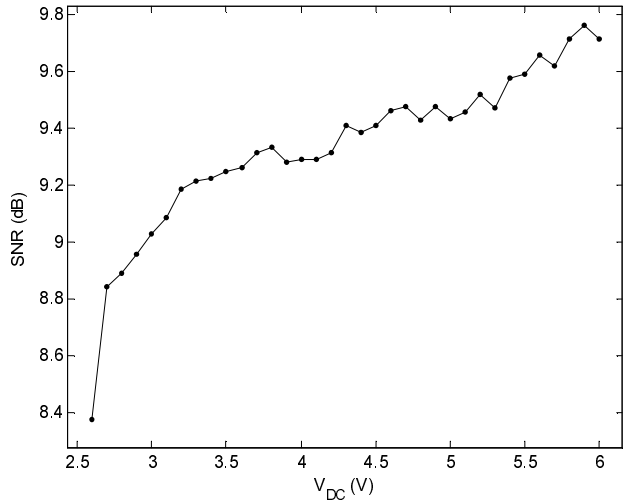

Figure 4.22. Receiver specification variation: modulation SNR.

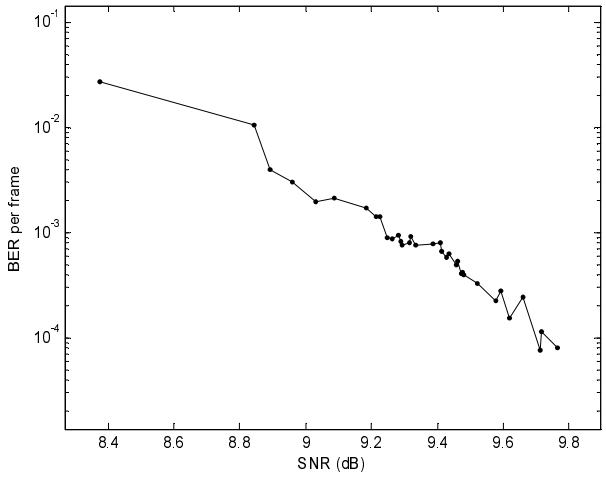

Figure 4.23. Receiver specification variation: BER vs. SNR.

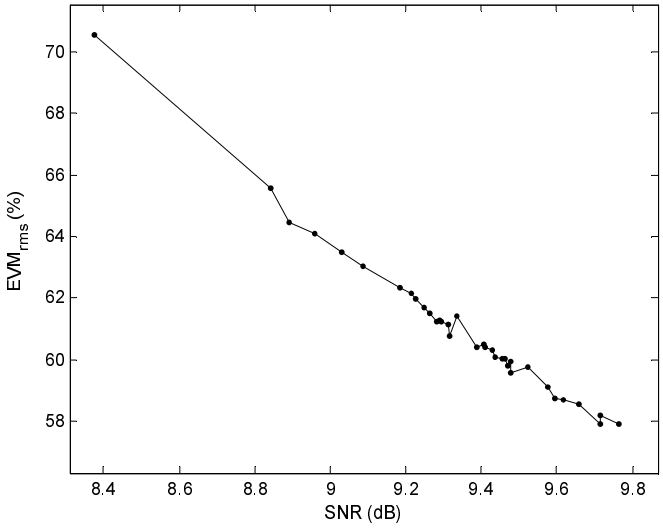

Figure 4.24. Receiver specification variation: EVM vs. SNR.

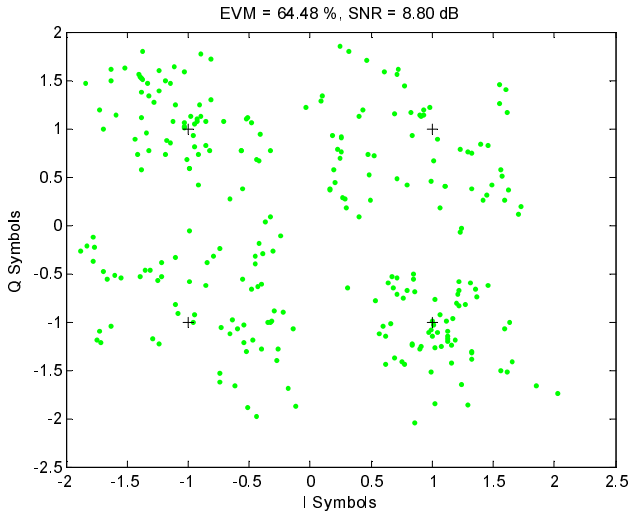

Figure 4.25. Symbol constellation for a data-frame consisting of 550 symbols: SNR=8.8 dB and EVM=64.5%.

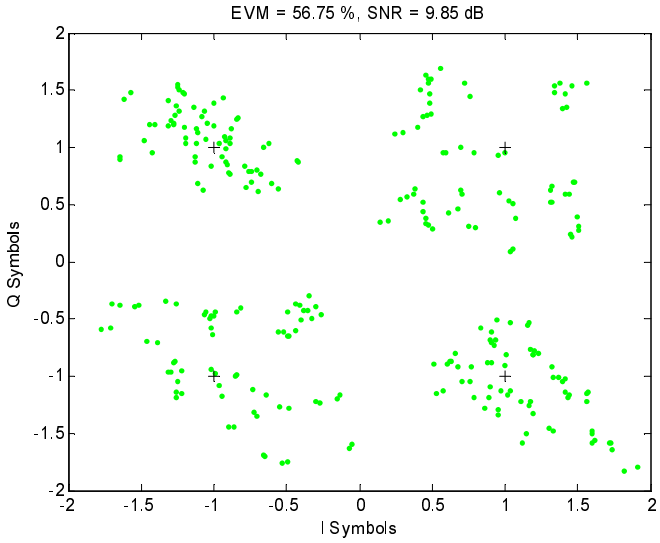

Figure 4.26. Symbol constellation for a data-frame consisting of 550 symbols: SNR=9.9 dB and EVM=56.8%.

In the proposed alternate test method, a sequence of tone-pairs at -55 dBm are applied at RF input of the receiver under test. One tone is applied at a fixed frequency of 1575.1 MHz and the other tone is incremented with a Δf_T = 8 kHz, i.e. 1575.108 MHz, 1575.116 MHz, …

1575.148 MHz. The LO is applied at 1575 MHz. At each step, the received baseband waveform is demodulated after recovering the carrier at 100 kHz. The test response spectra obtained corresponding to each test-node (see Figure 4.9) and each Δf_T step are concatenated to construct the measurement space, $\boldsymbol{M}$, (Section 4.3) for alternate testing. The end-to-end receiver specifications are predicted using the regression equations $f:\boldsymbol{M}\rightarrow\boldsymbol{S}$. Figure 4.27, Figure 4.28 and Figure 4.29 show the tracking of predicted BER and EVM specification values w.r.t. the corresponding measured values.

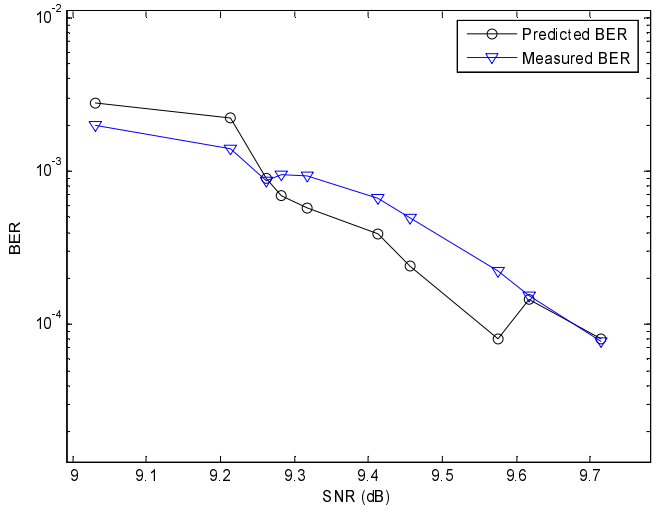

Figure 4.27. Specification tracking of predicted BER w.r.t different SNR values (across multiple receiver instances).

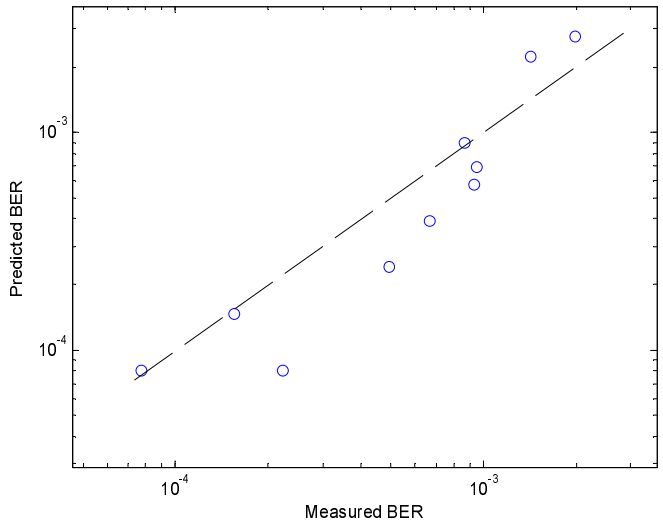

Figure 4.28. Specification tracking of predicted BER vs. measured BER.

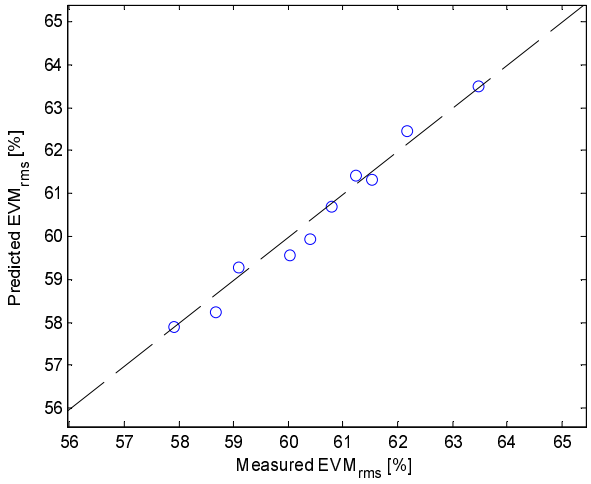

Figure 4.29. Specification tracking of predicted EVM vs. measured EVM.

It may be noted that, if there exists an accurate tracking the of the measured specification values (obtained from long conventional tests) by the predicted specification values (obtained from shorter alternate tests), the short alternate tests may be used to perform the end-to-end receiver specification tests at lower cost. The sources of error in the experimental results presented in Figure 4.27 through Figure 4.29 are:

1. The high noise floor (measured to be approximately -65 dBm) of the baseband A/D affecting the accuracy and the repeatability of the alternate test response digitization. For example, at -55 dBm input power level, third order intercept tones are below the A/D noise floor and can not be measured using the measurement setup (setup B) described in Figure 4.19.
2. The limited number (110k) of symbols used in standard method BER computation, which affects the accuracy of the computed regression model $f: \boldsymbol{M} \rightarrow \boldsymbol{S}$. A larger number of data-frames will improve the accuracy of BER prediction.

Case study II:

The experiment shown in the previous case study, which used the test condition of -55 dBm RF input signal level, is repeated for -20 dBm RF input power level. In this case, no bit-error occurs in the received data-frames because of the highly improved modulation SNR. At this RF input power level, the end-to-end receiver specifications are dominated by the nonlinearity effect of the receiver submodules. Figure 4.30 through Figure 4.36 show the receiver specifications for many receiver instances generated by varying the RF front-end supply voltage, viz. gain, noise figure, modulation SNR, EVM, symbol magnitude error, and symbol phase error of the receiver-under-test. The variation of EVM w.r.t. modulation SNR is shown in Figure 4.37. Figure 4.38 shows an example of symbol constellation corresponding to a received data-frame for SNR of 20.4 dB.

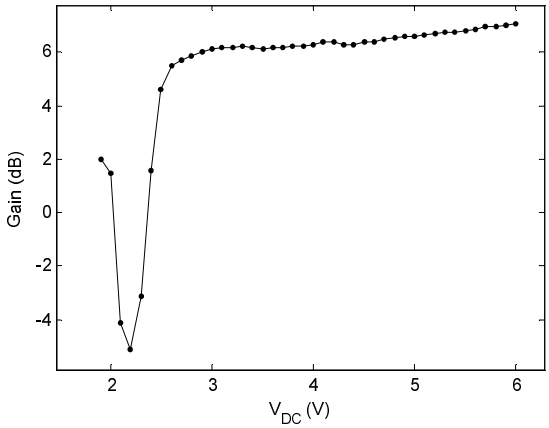

Figure 4.30. Receiver specification variation: receiver gain.

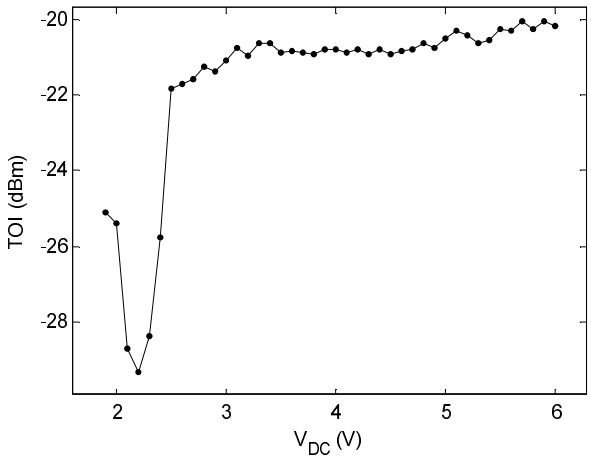

Figure 4.31. Receiver specification variation: receiver third-order-intercept.

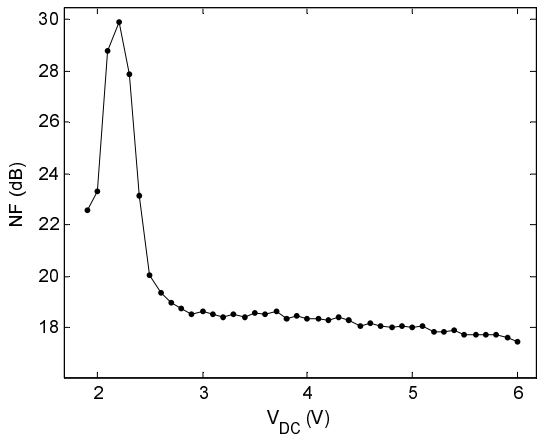

Figure 4.32. Receiver specification variation: receiver noise figure.

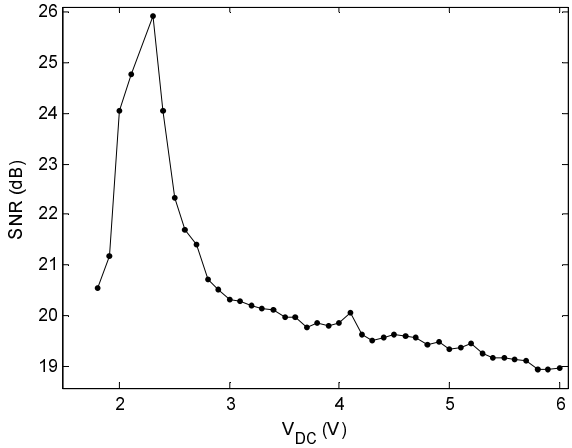

Figure 4.33. Receiver specification variation: modulation SNR.

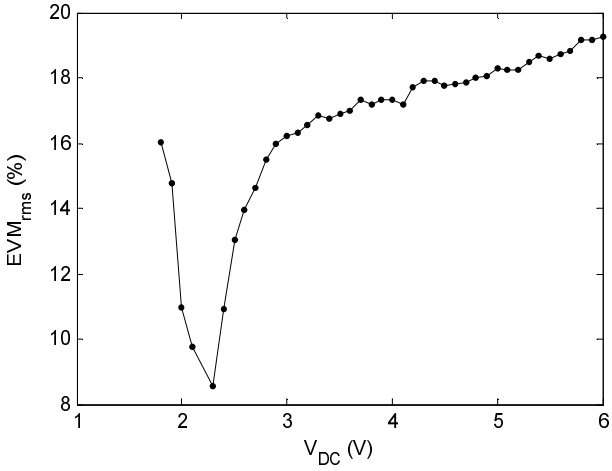

Figure 4.34. Receiver specification variation: EVM.

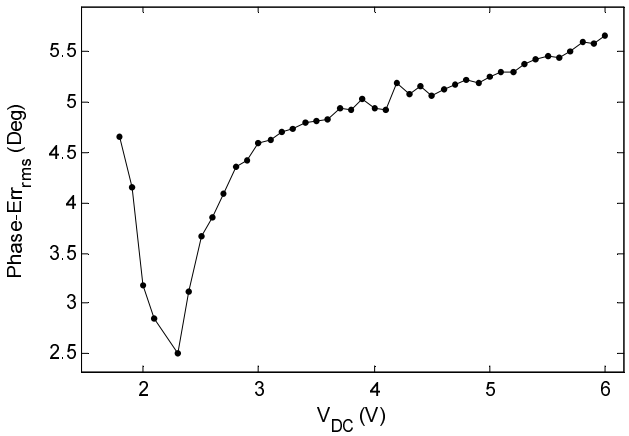

Figure 4.35. Receiver specification variation: r.m.s phase error in symbol constellation.

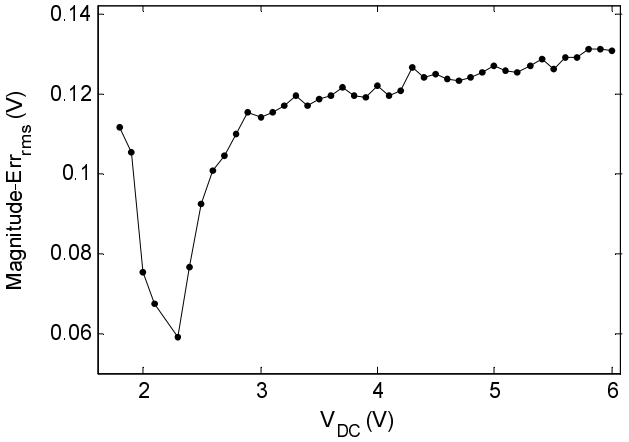

Figure 4.36. Receiver specification variation: r.m.s magnitude error in symbol constellation.

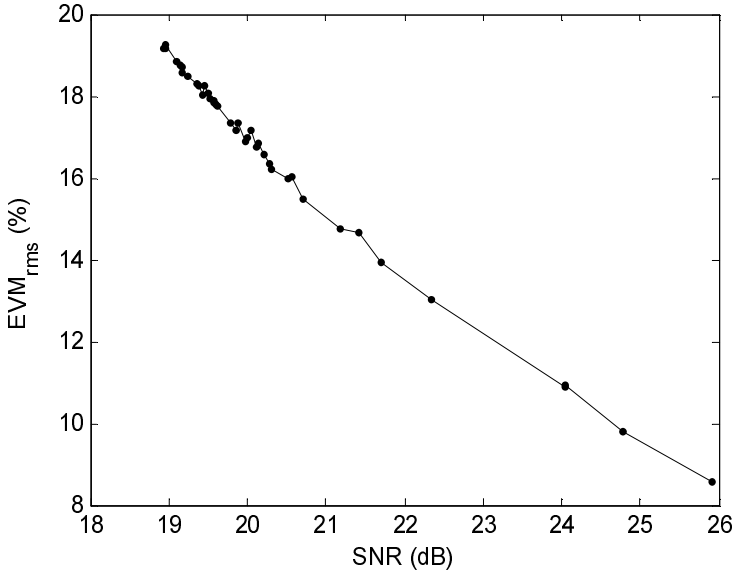

Figure 4.37. Receiver specification variation: EVM vs. SNR.

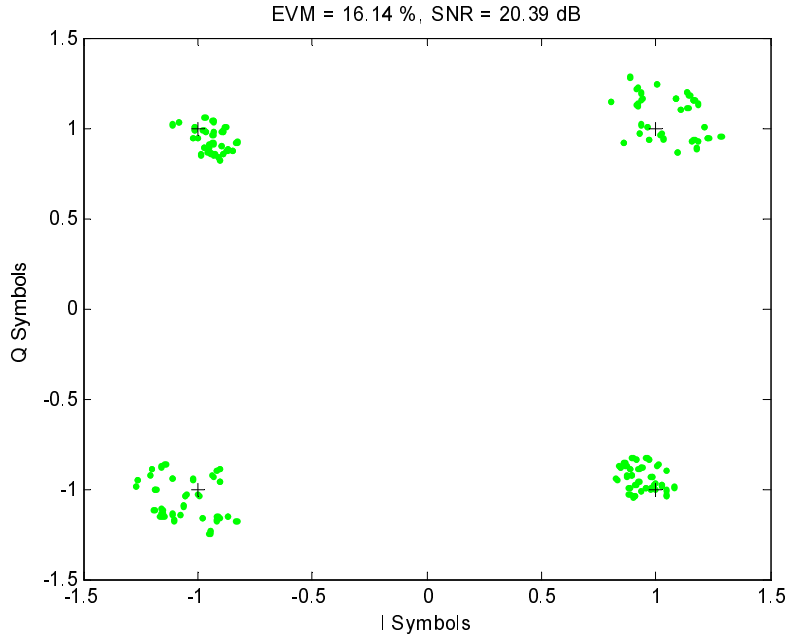

Figure 4.38. Symbol constellation for a data-frame consisting of 550 symbols: SNR=20.4 dB and EVM=16.1%.

A sequence of tone-pairs at -20 dBm is applied at RF input of the receiver-under-test. Similar to the previous case-study, one tone is applied at a fixed frequency of 1575.1 MHz and the other tone is stepped at Δf_T = 8 kHz, i.e. 1575.108 MHz, 1575.116 MHz, … 1575.148 MHz. The LO is applied at 1575 MHz. At each step, the received baseband waveform is demodulated after recovering the carrier at 100 kHz. The measurement space, ***M***, (Figure 4.39) for alternate testing is constructed by concatenating the test response spectra obtained corresponding to each test-node (Figure 4.9) and each Δf_T step. The receiver specifications are predicted using the regression equations f:***M***→***S***. Figure 4.40 through Figure 4.46 show the tracking of the measured specification values by the predicted specification values for gain, noise figure, SNR, EVM, symbol phase error and symbol magnitude error, respectively.

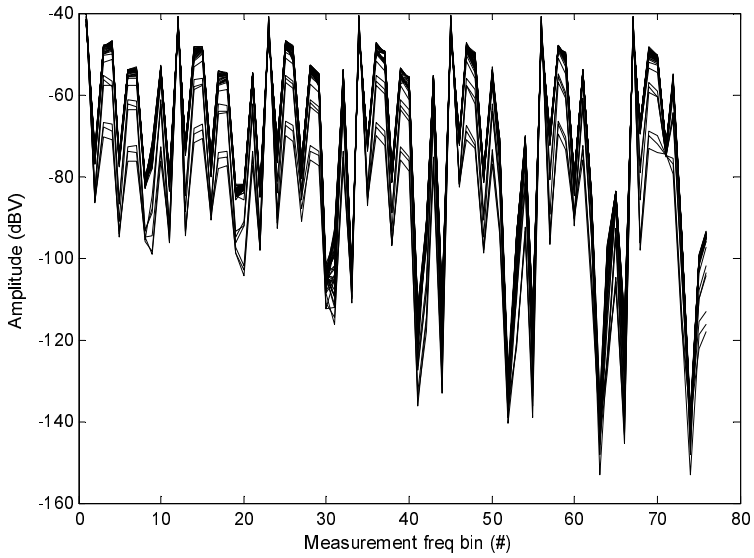

Figure 4.39. Frequency-domain alternate test measurement space for 42 different receiver instances.

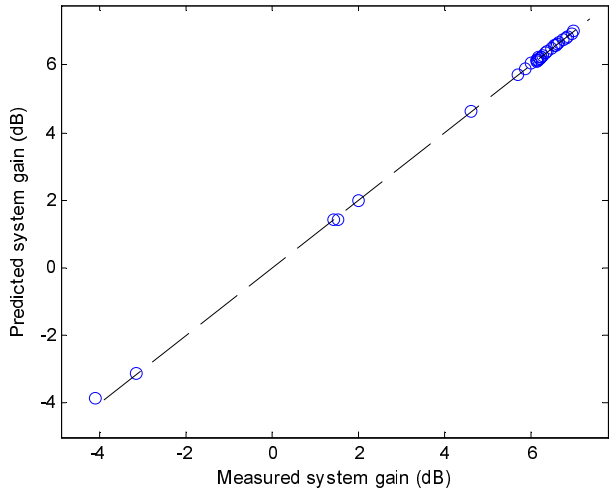

Figure 4.40. Specification tracking of predicted gain vs. measured gain.

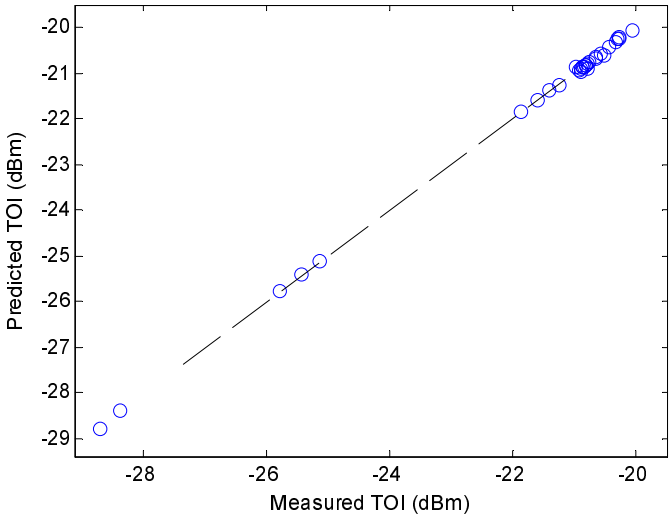

Figure 4.41. Specification tracking of predicted TOI vs. measured TOI.

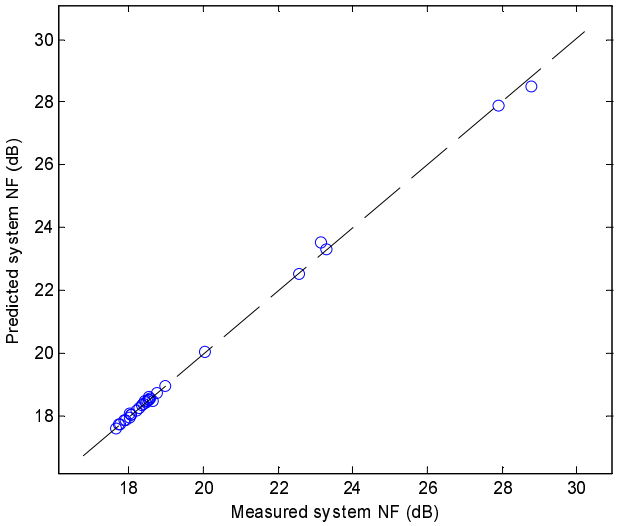

Figure 4.42. Specification tracking of predicted NF vs. measured NF.

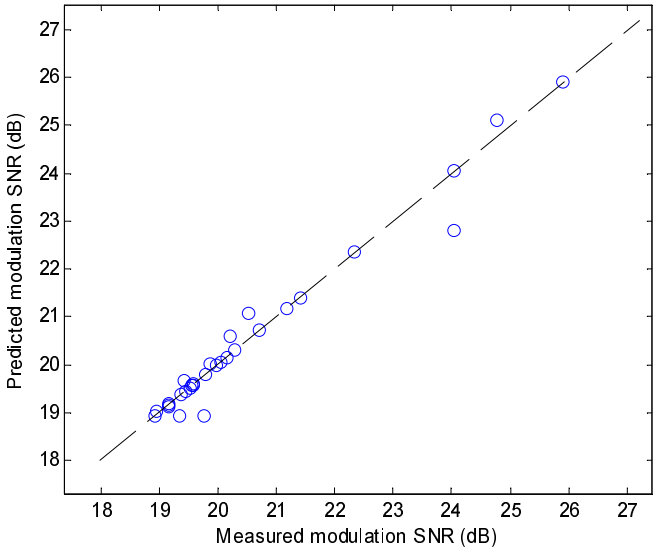

Figure 4.43. Specification tracking of predicted SNR vs. measured SNR.

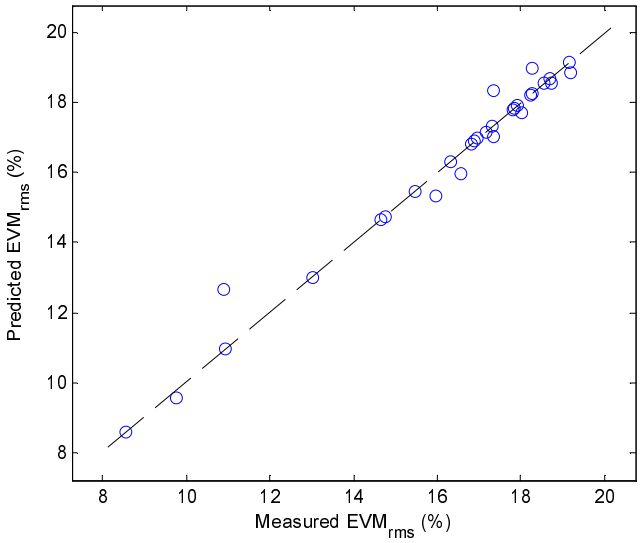

Figure 4.44. Specification tracking of predicted EVM vs. measured EVM.

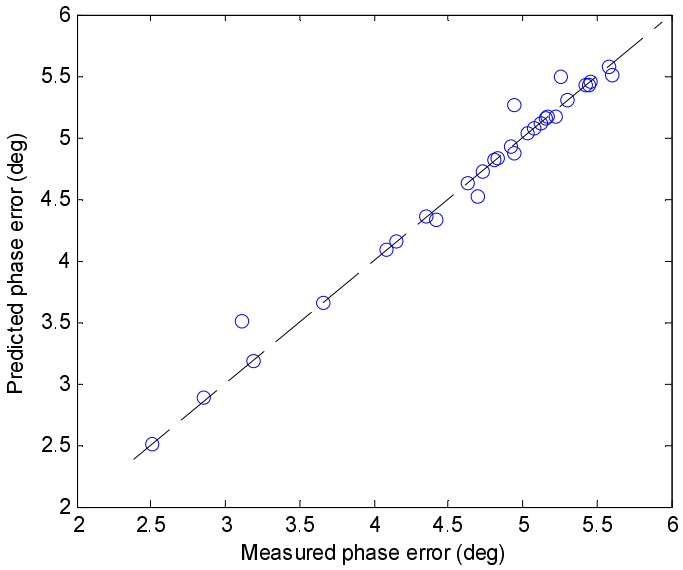

Figure 4.45. Specification tracking of predicted r.m.s. symbol phase error vs. measured r.m.s. symbol phase error.

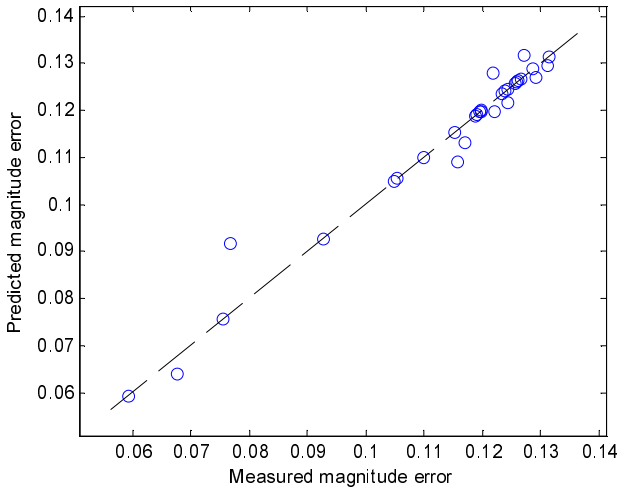

Figure 4.46. Specification tracking of predicted r.m.s. symbol magnitude error vs. measured r.m.s. symbol magnitude error.

The experimental results show that for the test condition of -20 dBm RF input power level, the proposed alternate test methodology can successfully replace the long, conventional specification tests and it can significantly reduce the production test cost for RF receivers.

Table 4.1 compares the prediction accuracy values obtained in alternate testing with that of conventional testing methodology for the test instrumentation used in the above experiment. It should be noted that the conventional specification measurement accuracy values for complex specifications, e.g. EVM, are not specified in the instrumentation datasheet [25]. For complex specifications, these accuracy values are derived from more fundamental instrumentation specifications, e.g. measured SNR in A/D or D/A [25]. For modulation-domain specifications, apart from the specification of the test instrumentation, the accuracy of phase-frequency detection of the digital-IF carrier in DSP affects the accuracy of the conventional specification testing. In Table 4.1, we assumed that the captured symbol magnitude-accuracy is primarily determined by the measurement noise of the A/D card. The accuracy of symbol phase-error was primarily determined by the phase-recovery

uncertainty due the finite number of waveform-samples (40 samples) within every cycle (0-2π) of the 100 kHz digital-IF carrier, followed by the finer reduction (by a factor of 0.08-0.1) in phase-error obtained using the constellation rotation algorithm. The corresponding uncertainty (after constellation rotation) in the computed values of EVM and SNR represents the accuracy of EVM and modulation-SNR test in conventional testing method. Table 4.1 shows that there is a little loss in specification test accuracy when using short and single alternate test instead of multiple and long conventional tests. Using more number of tone-pairs the accuracy of the specification prediction of the alternate test can be improved further at the expense of increased testing-time.

Table 4.1. Specification test accuracy comparison.

Specification	**| Max. prediction error | in alternate testing**	**| Accuracy | of conventional testing**
Gain	0.27 dB (Figure 4.40)	0.2 dB
TOI	0.68 dBm (Figure 4.41)	0.5 dBm
NF	0.42 dB (Figure 4.42)	0.2 dB
EVM_{rms}	1.75 % (Figure 4.44)	0.28 %
Magnitude error	14.9e-3 (Figure 4.46)	2.81e-3
Phase error	0.40 deg (Figure 4.45)	0.9 deg
Modulation SNR	1.26 dB (Figure 4.43)	0.1 dB

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CHAPTER 5

SYSTEM-LEVEL SPECIFICATION TESTING OF WIRELESS TRANSMITTERS

In the previous two chapters, low-cost alternate testing of wireless receivers has been described. In this chapter, the concept of alternate testing is demonstrated for specification testing of wireless transmitters.

5.1. Production Testing Problems for RF Transmitters

Production testing of modern wireless transmitters involves significant testing cost. The primary reasons for the high testing cost are:

1. Long test times necessary for some of the system-level transmitter specifications
2. Test-time and test-instrumentation overhead of using different test-hardware setups for different system-level specifications.

For example, adjacent-channel-power-ratio (ACPR) [1] is a frequency-domain "out-of-band" transmitter specification. The conventional method of ACPR testing requires a long modulated bit-sequence to be transmitted from the transmitter baseband and the spectral test response to be observed at its RF output. The conventional testing approach for error-vector-magnitude (EVM) also requires a lengthy bit-sequence be used as test stimulus, while its test response is analyzed by an 'ideal' receiver embedded in RF automated test equipment (ATE) [2]. Although ACPR and EVM testing use long modulated bit sequence as the test stimulus at

low baseband data rate, it is not feasible to merge the ACPR test and the EVM test into a single test in the standard test methodology because of the difference in the required test hardware setups.

In this chapter, a new production test methodology has been proposed using which multiple frequency-domain specification tests and modulation-domain specification tests for wireless transmitters can be tested simultaneously using a single test. Using the proposed alternate testing technique, the overall testing time for production testing of wireless transmitter can be reduced significantly. The key contributions of the proposed methodology are as follows.

1. The modulation-domain system-level specifications are measured using frequency-domain testing methods. In the past, techniques for estimating the EVM of power amplifiers ([3], [4]) using their spectral response have been investigated. For a complete transmitter, no such work has been reported in the literature.
2. All the frequency-domain and the modulation-domain specifications are measured using a single test.

As a consequence, the primary benefits obtained from using the proposed methodology for production testing of wireless transmitter are as follows:

1. Multiple system-level, complex transmitter specifications are tested using a short, single test.
2. The proposed testing methodology simplifies the test hardware complexity by eliminating the need for using separate test hardware setups for multiple specifications.

Experimental results using a 1.575 GHz wireless transmitter prototype shows a significant reduction in the overall testing time for wireless transmitters.

5.2. System Specifications of a Wireless Transmitter

Multiple frequency-domain and modulation-domain system specifications of a wireless transmitter are tested simultaneously using the proposed alternate testing methodology. In this chapter, the proposed technique has been demonstrated for the following system-level specifications:

Frequency-domain in-band/out-of-band specifications:

1. System gain
2. Output third-order-intercept (TOI or OIP3)
3. Channel power
4. Lower and upper adjacent channel power ratio (ACPR).

Modulation-domain specifications:

1. Error vector magnitude (EVM)
2. Magnitude error
3. Phase error
4. Modulation signal-to-noise ratio (SNR)

In [1], [2], [5], and [6], the basics of conventional measurement and testing methods for these specifications are discussed. System gain and system OIP3 are measured using two-tone tests (Figure 5.1). For a specified RF power level condition, a two-tone waveform is applied from baseband and spectral response is observed at the RF output using spectrum analyzer. If each of the two baseband tones are at power level P_{in} (in dBm), the system gain and system OIP3 are given by Equation (5.1) and Equation (5.2).

$$\text{Gain (in dB)} = P(f_2) - P_{in}, \text{ and} \quad \textbf{(5.1)}$$

$$\text{OIP3 (in dBm)} = P(f_2) + \Delta P/2, \text{ where } \Delta P = P(f_2) - P(2f_2 - f_1), \quad \textbf{(5.2)}$$

In ACPR and channel power testing, for the same specified output power level, a modulated bit sequence from baseband is applied as the stimulus. Corresponding RF spectrum is observed at the transmitter output (Figure 5.2). At the RF output, for a given channel bandwidth and the given frequency spacing between adjacent channels (specified by the wireless communication standard), the in-channel, lower-adjacent channel and upper-adjacent channel power values are measured. If $P_{Channel}$ and $P_{lower\text{-}channel}$ ($P_{upper\text{-}channel}$) are the in-channel power and the lower-adjacent channel power, $ACPR_{lower}$ ($ACPR_{upper}$) is computed using Equation (5.3).

$$ACPR_{lower} \text{ (in dBc)} = P_{Channel} - P_{lower\text{-}channel} \quad \textbf{(5.3)}$$

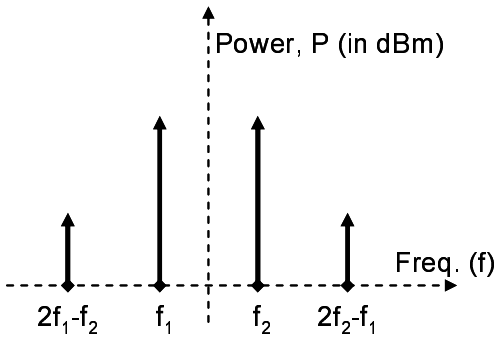

Figure 5.1. Gain and TOI using two-tone stimulus.

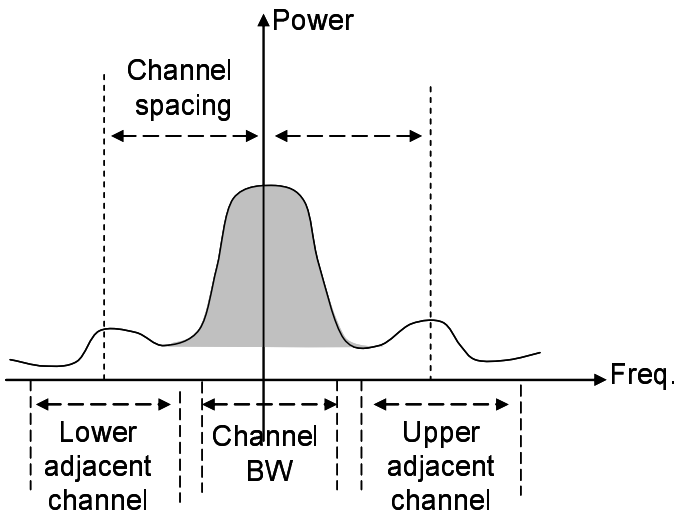

Figure 5.2. Channel power and ACPR (lower and upper) using modulated bit-sequence stimulus.

Testing of modulation-domain specifications defined at the transmitter RF output, e.g. EVM, magnitude and phase errors in symbol constellation (Figure 5.3), modulation SNR (Figure 5.4), require down-conversion and demodulation of the modulated RF spectrum using an 'ideal' receiver of in the ATE. Error vector magnitude is computed as,

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{1}^{N} \|R - S\|^2}{\|S_{max}\|^2}} \qquad \textbf{(5.4)}$$

where,

R = the received symbol in vector form (I + jQ),

S = the reference symbol in vector form (I + jQ),

S_{max} = the outermost symbol in the constellation diagram,

N = number of symbols used for EVM computation, where N is sufficiently large.

Because of the statistical nature of the specifications related to symbol constellations, many data-frames consisting of pseudo-random bit sequences must be applied as test stimuli.

Table 5.1 presents a summary of the test time and the test instrumentation needed for these specification tests. It should be noted that the exact values of testing times are dependent on the specific system-under-test, i.e. its baseband data-rate and RF bandwidth. Hence, the 'relative testing time' impact across these specification tests are shown in Table 5.1. For example, the two-tone test is the shortest test, whereas the tests using modulated bit-sequence incur significantly longer testing time. With the core testing concepts for these specifications in mind, this chapter focuses on a low cost test approach for these specifications in a manufacturing environment.

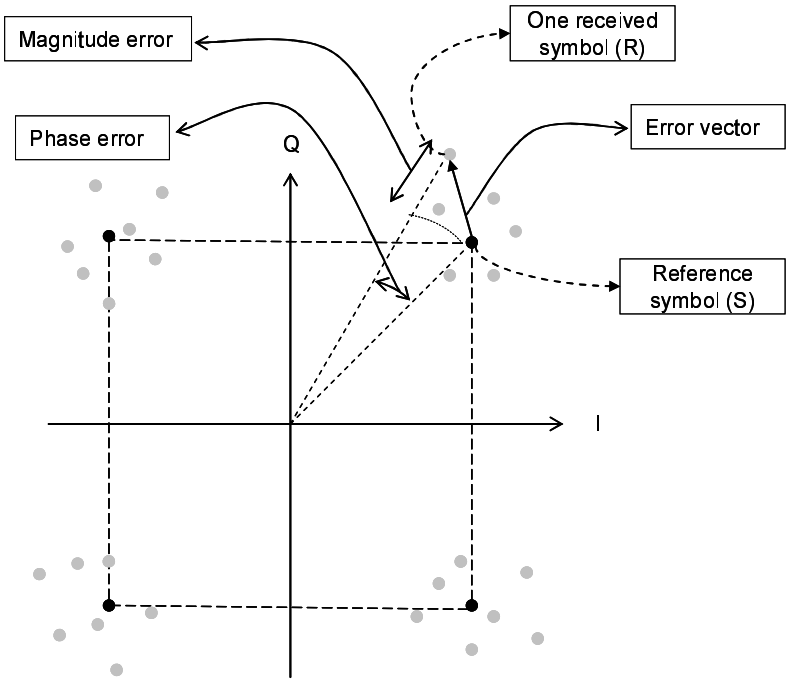

Figure 5.3. Modulation domain transmitter specification: EVM, magnitude error, phase error.

In the proposed alternate test methodology for wireless transmitter, large-signal multitone sinusoids applied from the transmitter baseband replaces any other stimuli used in Table 5.1. A spectrum analyzer is used for capturing the RF spectral test response. The RF

test response spectrum is analyzed to accurately predict all the transmitter specification using the *alternate testing* framework. Pass/fail decisions for the production tests are made using the predicted spcification values. The basic concept of alternate testing is discussed next.

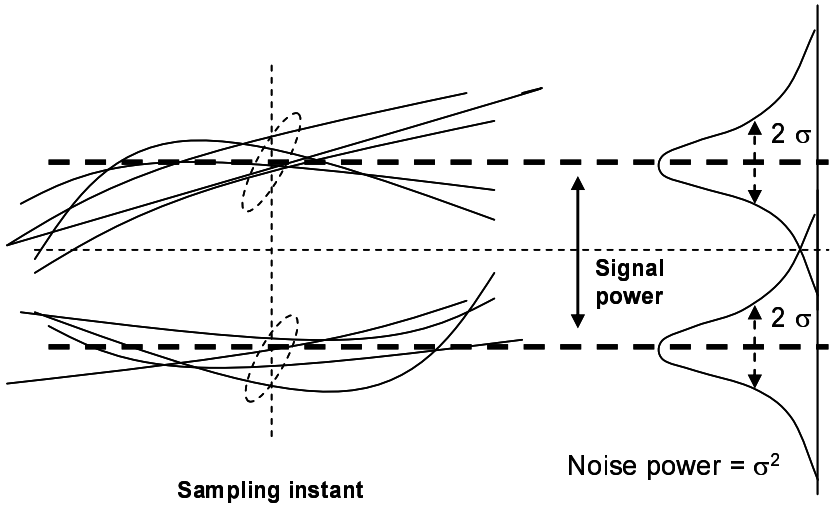

Figure 5.4. Modulation domain transmitter specification: SNR.

Table 5.1. Summary of test time impact in conventional test of wireless transmitter.

Specification	Stimulus	Test response	Test H/W requirement	Primary test time impact	Relative test cost	
1. System gain 2. TOI	Two-tone	RF Spectrum	Spectrum analyzer	Frequency sweeping over the measurement frequency-span	low	Figure 5.1
3. Channel power 4. ACPR's	Data-frames consisting of modulated bit-sequence				high	Figure 5.2
5. EVM 6. Magnitude error 7. Phase error		Constellation of demodulated symbols	Ideal receiver	Demodulation of large number of symbols	high	Figure 5.3
8. Modulation SNR		Eye-diagram of demodulated symbols			high	Figure 5.4

5.3. Basic Concepts

As shown by the past research work ([7], [8]) on specification based test generation, variation of any circuit parameter and process parameter in the parameter space (Figure 5.5) alters the circuit specifications ($\boldsymbol{S}$ = {S_1, S_2, …}) by a corresponding sensitivity factor. The variation in process parameters also affects the measurement data ($\boldsymbol{M}$ = {m_1, m_2 …}) in the measurement space of the circuit by a corresponding sensitivity factor.

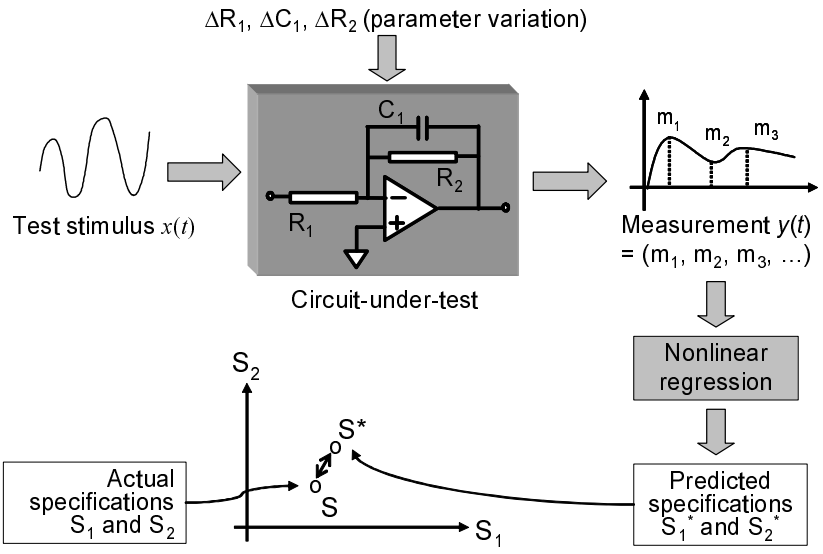

Figure 5.5. Process parameter variation and its effect on specification and measurement.

The work reported in [7] and [8] showed that, for a carefully selected test stimulus, mapping functions, $\boldsymbol{f:M \rightarrow S}$, can be constructed for each specification using regression analysis, which map the measurement space information (test response data) onto the specification space. Given the existence of the regression mapping function $\boldsymbol{f:M \rightarrow S}$, using the selected stimulus, an unknown specification value of a circuit-under-test can be predicted

under the same process variation conditions. The stronger the statistical correlation between the parameter space and the measurement space, the more accurate the prediction of specification. The selected 'alternate test' can then be used to reduce the test time for individual tests, or to simplify the test hardware requirement, or to combine multiple tests into a fewer number of tests and so on.

The proposed test methodology uses the above alternate testing framework and applies it to perform specification testing of a complete RF transmitter. In the proposed approach, the measurement space (***M***) consists of the RF spectral responses observed at the output of the transmitter corresponding to the multitone test stimulus waveform. As shown in the experimental results, both modulation-domain and frequency-domain specifications are strongly correlated with the RF test response spectrum so that the test response spectrum can be used to predict all the transmitter specification values at once. Multivariate Adaptive Regression Splines (MARS) [9] are used to compute the regression model and estimate the transmitter specifications using the RF test response spectrum.

The goal of the proposed approach is to select an optimal multitone test stimulus waveform to be applied at the transmitter baseband for which high prediction accuracy for the transmitter specifications can be achieved.

5.4. Test Architecture

Figure 5.6 shows the architecture of the transmitter-under-test for executing the alternate test methodology. The large-signal sampled multitone test stimulus waveform is generated from the DSP and applied to the analog front-end using the built-in D/A converter. The spectral data of the test response at RF is captured using a swept-tuned spectrum analyzer.

The RF test response spectrum is used to predict all the frequency-domain and modulation-domain transmitter specifications using the alternate testing concept. In essence, the ATE setup for alternate testing is identical to the two-tone test used for conventional testing of system gain and nonlinearity (TOI).

The overall test-time is primarily determined by the frequency sweeping time of the spectrum analyzer. Since, both the frequency-domain and the modulation-domain specifications are tested using a single test stimulus, the overall test time is significantly reduced. The total test-time is marginally longer than a conventional two-tone test and is significantly shorter than any of the conventional tests that use modulated bit sequence stimuli.

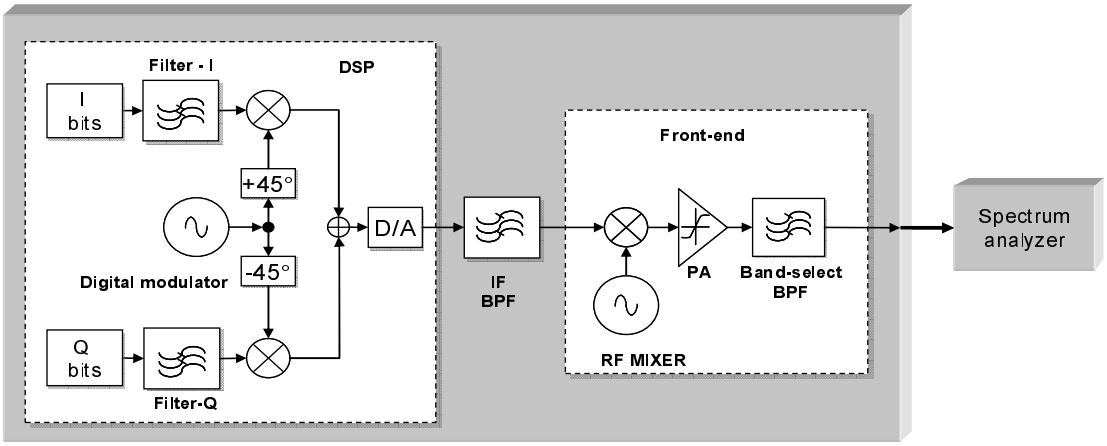

Figure 5.6. Test architecture for alternate testing.

5.5. Test Stimulus Selection

The choice of test stimulus type (e.g. sinusoids, periodic or pseudo-random bit sequence, etc.) and the corresponding test stimulus waveform parameters are primarily dictated by:

1. the specifications of the spectrum analyzer, e.g. resolution bandwidth, amplitude dynamic range.
2. the specification of the transmitter components, e.g. full-scale range, number of bits, waveform buffer limitations of the baseband D/A; the input dynamic-range of up-conversion mixer, PA and filters; the operating RF power-level at which the transmitter specifications are defined.

In the proposed alternate testing methodology, a large-signal multitone transient waveform is applied from the baseband as test stimulus. The waveform is of the form:

$$V(t_n) = A \cdot \sum_{k=1}^{N_t} V_k \cos(2\pi f_k n T_s + \phi_k), \quad n = 0 \cdots (N_s - 1) \tag{5.5}$$

where,

N_t = number of tones present in the test stimulus waveform applied from the baseband;

$\{f_k, V_k, \phi_k\}$ = the frequency, the peak-amplitude, and the phase of individual tone present in the multitone stimulus;

$1/T_s$ = sampling rate of the waveform.

A = factor to scale the peak-to-peak test stimulus signal incursion below the input dynamic ranges transmitter components and to operate at the RF output power-level at which specifications are to be production-tested.

Each tone at f_k is coherent w.r.t. the number of samples, N_s, used in the baseband D/A output buffer, i.e. $(N_s \cdot T_s \cdot f_k)$ is an integer for all k's. The coherence criterion prevents any amplitude discontinuity of the test stimulus waveform when it is applied repeatedly during the spectrum analyzer frequency sweeps. No spurious or non-repeatable tones appear at RF output during the test response capture (Figure 5.7).

The objective of the test generation algorithm is to select optimal N_t, N_s, A, and $\{f_k, V_k, \phi_k\}$'s so that the error in the specification values predicted by the regression function,

$f:M \rightarrow S$, using the RF test response spectrum is lower than a required error threshold (input to the algorithm).

1. Spectral measurement frequency span, F_{span} (dependent on RF channel bandwidth)
2. Minimum frequency spacing between adjacent tones, $F_{spacingv}$ (Figure 5.8) (dependent on the resolution bandwidth of spectrum analyzer)
3. Maximum amplitude for a tone, V_{max} (dependent on the max. input power handling of up-conversion mixer)
4. Minimum amplitude for a tone, V_{min} (dependent on D/A resolution)
5. Maximum number of samples in a waveform segment, $N_{s,max}$ (dependent on the maximum number of samples that can be buffered to the baseband D/A)
6. Minimum number of samples in a waveform segment, $N_{s,min}$ (dependent on min. number of samples that can be buffered to D/A for continuous waveform output, without zero padding. Zero padding results in amplitude discontinuity.)
7. Frequency coherence constraint
8. Specification prediction error threshold for each specification, ΔErr's

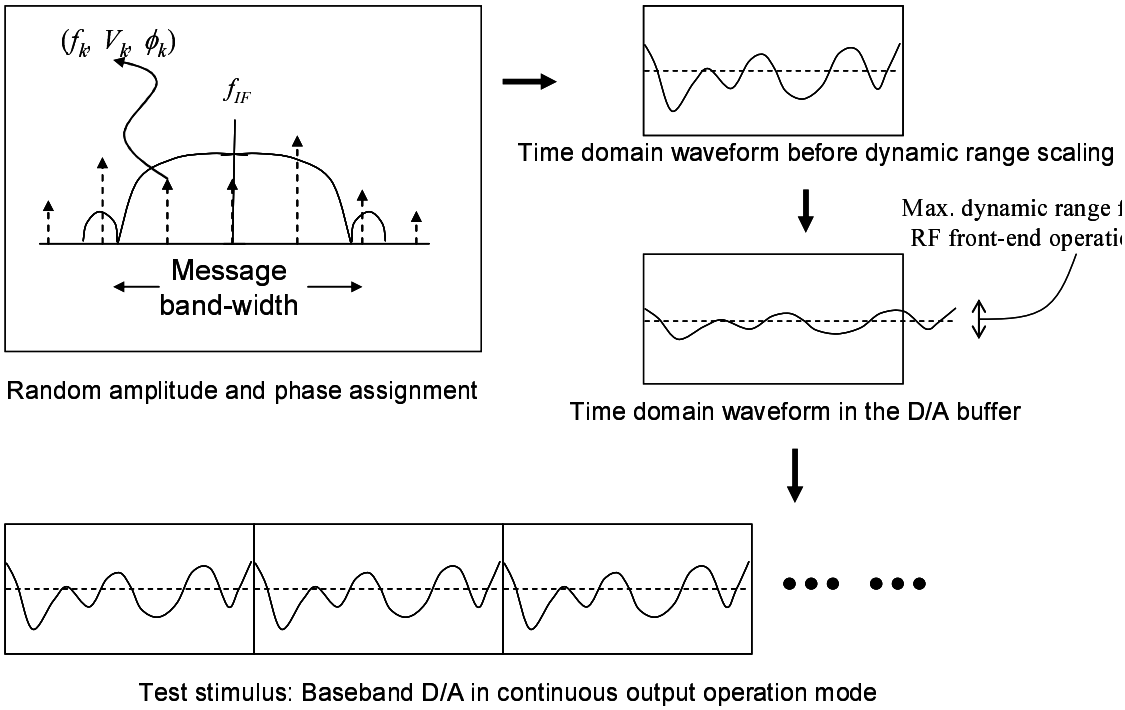

Figure 5.7. Multitone test stimulus applied in transmitter baseband.

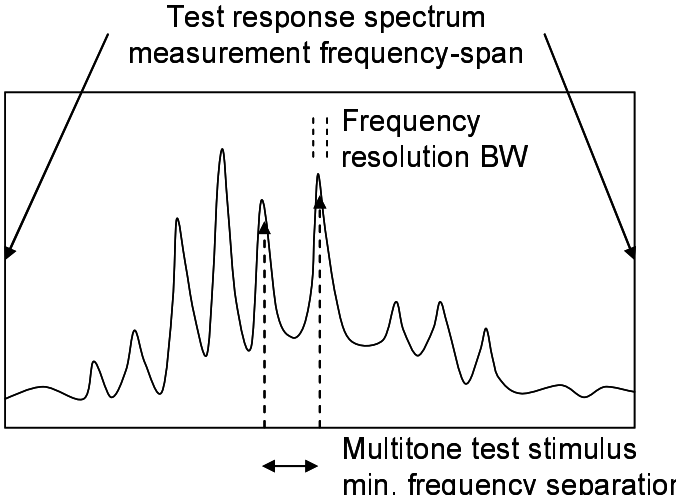

Figure 5.8. Spectral test response measurement at RF corresponding to multitone alternate test stimulus.

Behavioral-level system simulation [10] is used for fast test selection. It is observed in simulation that for a search space over $\{f_k, V_k, \phi_k\}$, average error in specification prediction shows no statistical trend over the test stimulus parameter space. Therefore, a greedy, random search technique is used to select $\{f_k, V_k, \phi_k\}$'s, with $N_s = N_{s,max}$ in Equation (5.5). A multitone waveform, which satisfies all of the above constraints for the given test hardware setup and gives specification prediction errors less than ΔErr's is selected as the test stimulus.

5.6. Experimental Results

A case study is presented below on which the proposed test methodology has been applied. A 1.575 GHz transmitter prototype was developed using off-the-shelf components, e.g. PA, RF filter, up-conversion mixer, on printed circuit board. The selection of front-end operating frequency was solely determined by the availability of the off-the-shelf RF components. The proposed methodology can be used for a different RF front-end frequency also.

In the conventional transmitter testing set-up, a spectrum analyzer (setup B of Figure 5.9) was used to measure the system gain, TOI, channel-power, ACPR. For EVM measurement, transmitter output was down-converted using off-the-shelf mixer and baseband filters (setup A of Figure 5.9). For the baseband operation, Matlab software was developed to interface the analog front-end via a data acquisition (DAQ) card operating at 4 Msamples/s having an effective-number-of-bits value (ENOB) of 11 bits. The Matlab software performs the required DSP functionality of the transmitter-under-test and also the ATE functionality of the receiver DSP, DAQ interface, test response data collection and analysis, and test-flow control. In the baseband DSP, a digital-IF (100 kHz) offset-quadrature-phase-shift-keying

(OQPSK) [11] modulation scheme was implemented, which is commonly used in W-CDMA standard. Baseband data-rate was 25kbps for each of I and Q channels. A data transmission frame size of 600 I-Q symbols was used, where the size was limited by the maximum buffer-size of the DAQ interface. RF channel bandwidth of 275 kHz and channel spacing of 300 kHz were assumed.

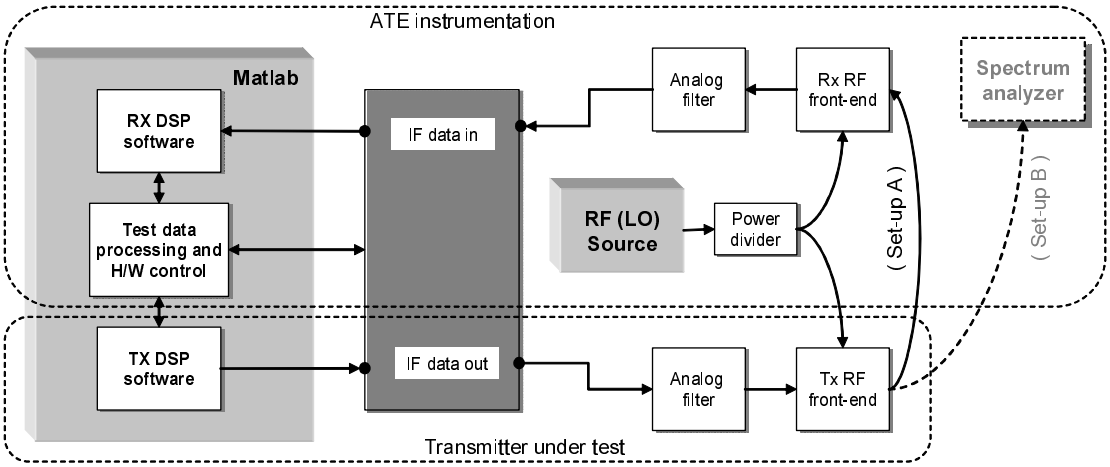

Figure 5.9. Transmitter prototype under test and ATE instrumentation.

To verify the proposed alternate test methodology, multiple instances of the transmitter design were generated by varying the supply voltage given to the active components of the RF front-end. The nominal operating supply-voltage was 3.0V. The supply voltage to the front-end devices was varied from the minimum of 1.7V (below which the devices do not turn on) to the maximum of 6.0V (highest absolute rating) to generate a wide range of different specification values. It should be noted that generation of multiple instances of the transmitter-under-test can also be achieved by using multiple instances of devices via test-sockets. However, the generation of multiple transmitter instances by supply voltage variation had the following advantages:

1. The range of variation in specification values of the transmitter-under-test is much larger than the range of variation obtained using multiple (good) components commercially available. Larger specification variations present a worse case scenario for a testing methodology relying on prediction of specifications.
2. A test socket provides a source of random variability into the measurement system.

Figure 5.10 shows an example of the output 1.575 GHz RF spectrum of the transmitter-under-test corresponding to a data-frame containing OQPSK modulated pseudo-random bit sequence. Figure 5.11 shows the corresponding symbol constellation after down-conversion of the RF output and subsequent demodulation of the data-frame symbols.

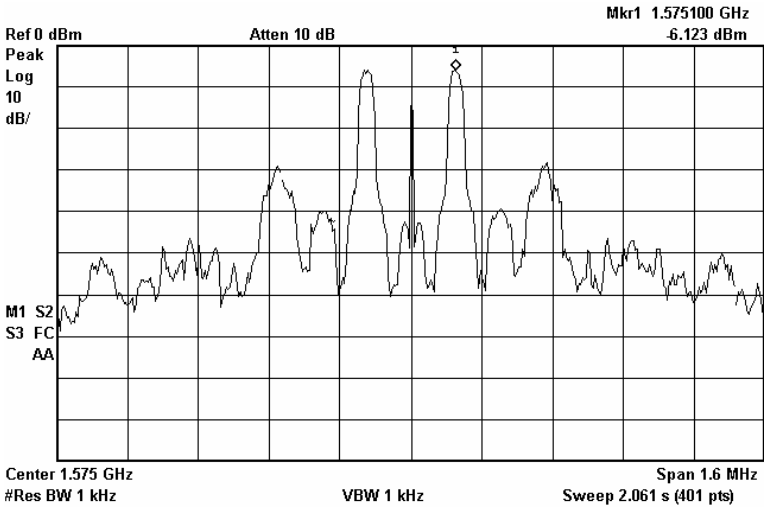

Figure 5.10. Output RF spectrum example.

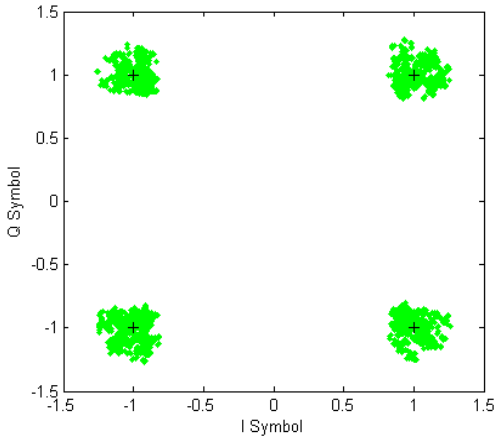

Figure 5.11. Symbol constellation for Figure 5.10. EVM_{rms} = 13.8%, Modulation SNR = 21.7dB, rms magnitude error = 0.11, rms phase error = 3.6deg, front-end supply=3.0V.

Figure 5.12 through Figure 5.19 show the transmitter specification variation corresponding to the supply voltage variation. The specifications were system-gain, TOI, channel power, lower adjacent channel power ratio, modulation SNR, rms values of EVM, magnitude error and phase error, respectively.

Using the random test stimulus selection approach a multitone test stimulus containing N_t = 9 coherent tones within 25 kHz to 125 kHz frequency span (i.e. F_{span} = 100 kHz) were selected. N_s = 32k samples ($N_{s,max}$) was selected for continuous mode DAQ card operation. Peak-to-peak signal incursion was limited to 10 dBm (50ohm reference) for the given input dynamic range of up-conversion mixer. The resulting multitone stimulus was applied from the baseband and test response spectrum was observed at the RF output. Figure 5.20 shows the ensemble of test response spectra for 44 transmitter instances. A subset from the ensemble of test response spectra were mapped onto the individual specifications using Multivariate Adaptive Regression Splines (MARS) [9] and the corresponding multivariate

regression models, $f:M \rightarrow S$, were computed. For another set of randomly selected unknown transmitter instances, individual specifications were predicted.

Figure 5.21 through Figure 5.28 show the specification tracking for all the specifications against the conventionally measured specification. It shows that the specification values predicted using alternate test methodology track the corresponding actual specification values (obtained using lengthy conventional tests), and fall closely along the straight line having slope +1 passing through origin. Hence, the alternate test set-up can replace different conventional test set-ups for testing transmitter specifications during production testing.

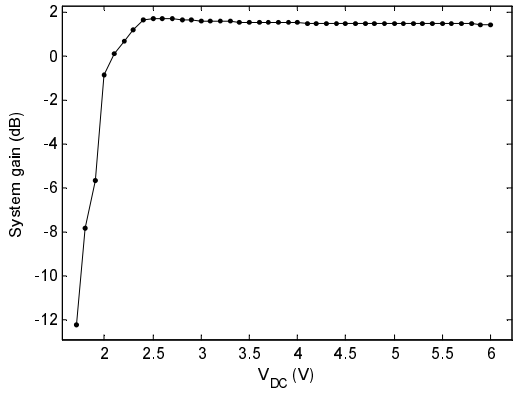

Figure 5.12. Specification variation for the transmitter-under-test: System gain.

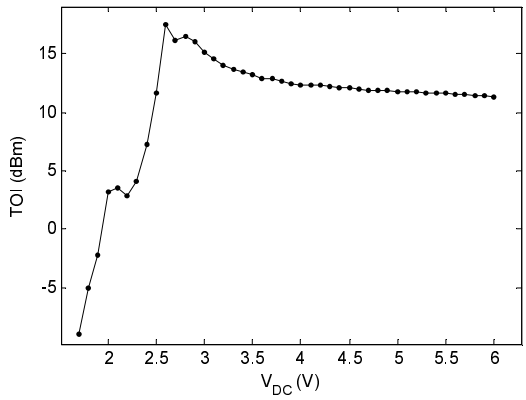

Figure 5.13. Specification variation for the transmitter-under-test: System TOI.

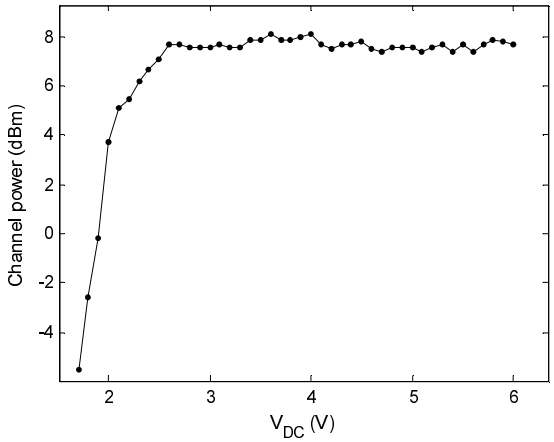

Figure 5.14. Specification variation for the transmitter-under-test: Channel power.

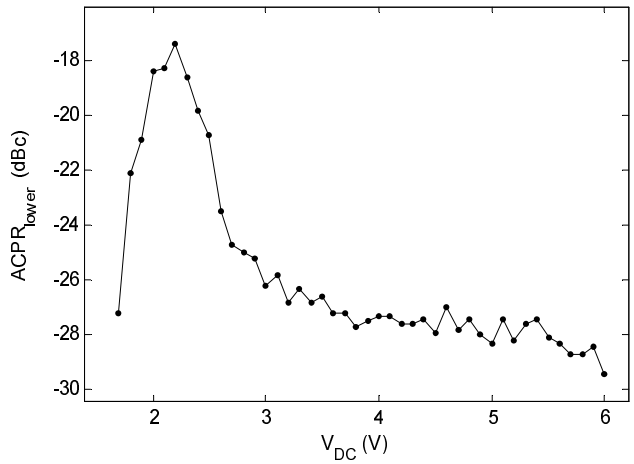

Figure 5.15. Specification variation for the transmitter-under-test: $ACPR_{lower}$.

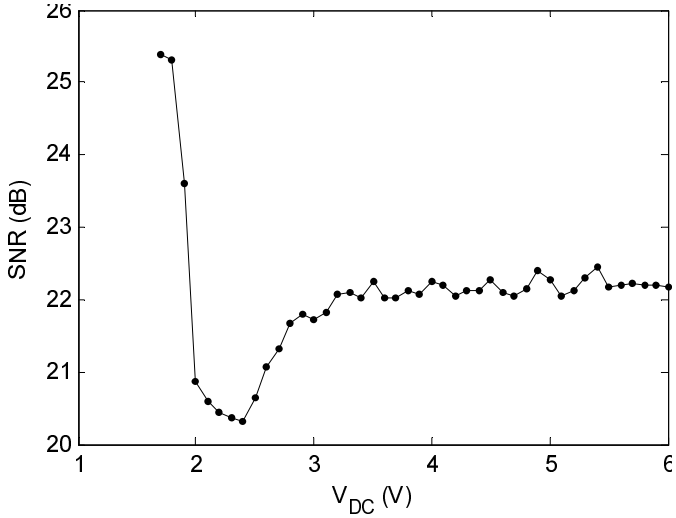

Figure 5.16. Specification variation for the transmitter-under-test: modulation-SNR.

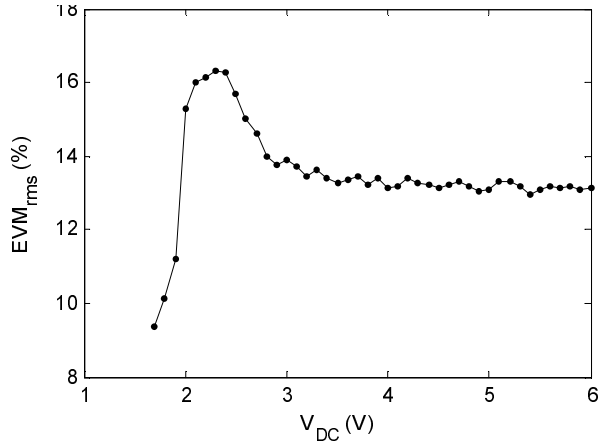

Figure 5.17. Specification variation for the transmitter-under-test: EVM_{rms}.

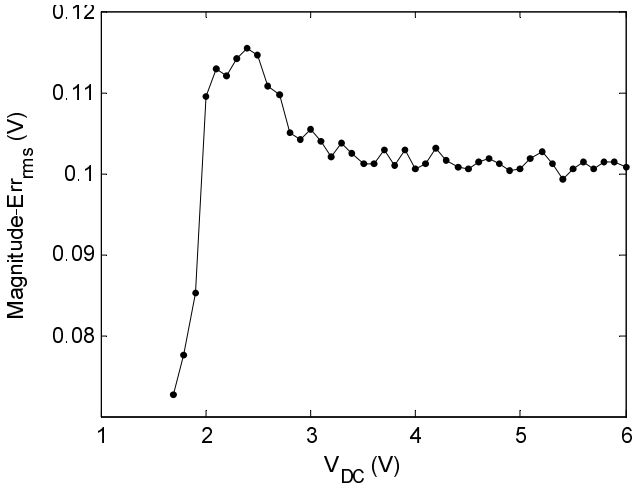

Figure 5.18. Specification variation for the transmitter-under-test: rms magnitude error.

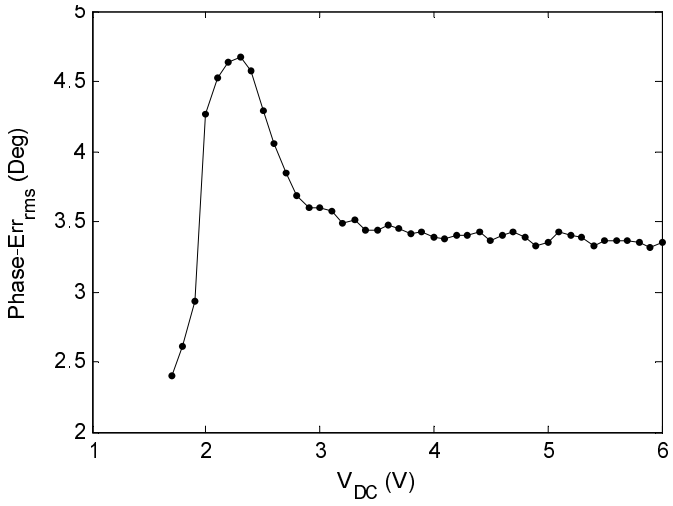

Figure 5.19. Specification variation for the transmitter-under-test: rms phase error.

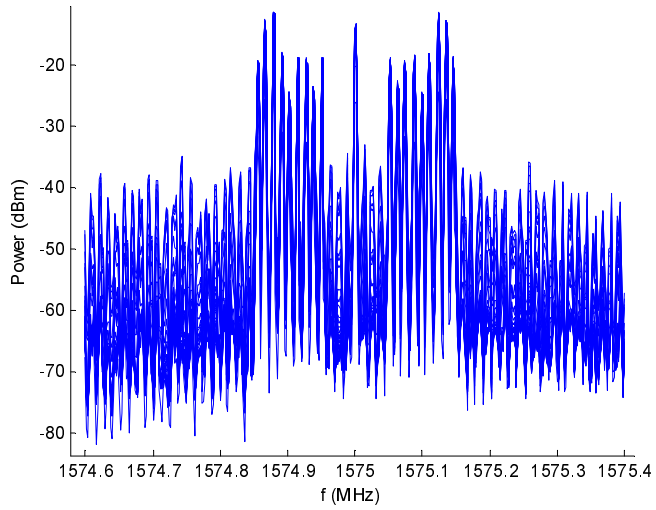

Figure 5.20. Measurement space (ensemble of test response spectra) corresponding to the alternate test stimulus under specification variations.

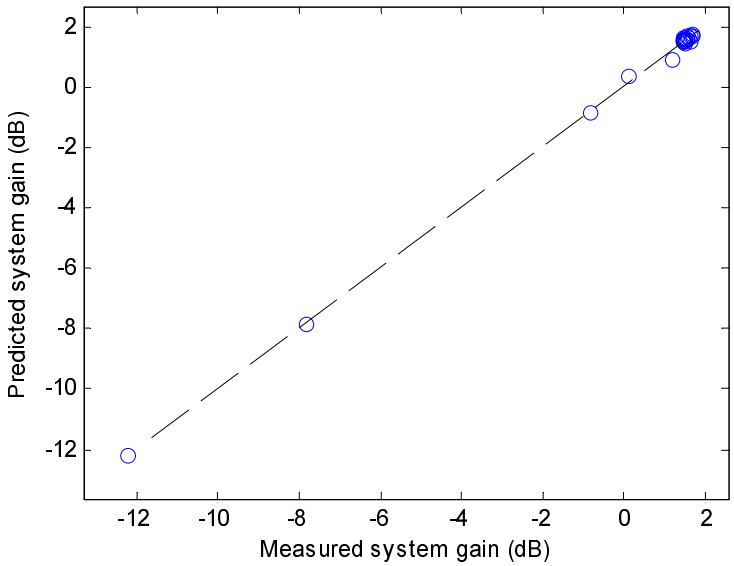

Figure 5.21. Specification tracking using alternate-test methodology: Gain.

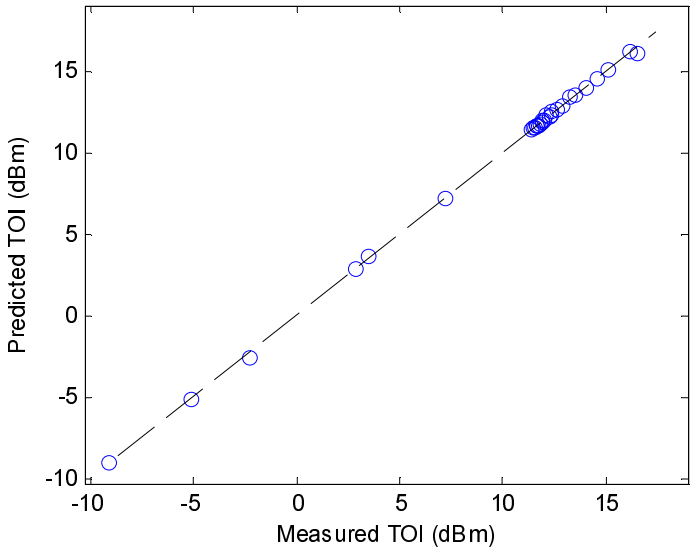

Figure 5.22. Specification tracking using alternate-test methodology: TOI.

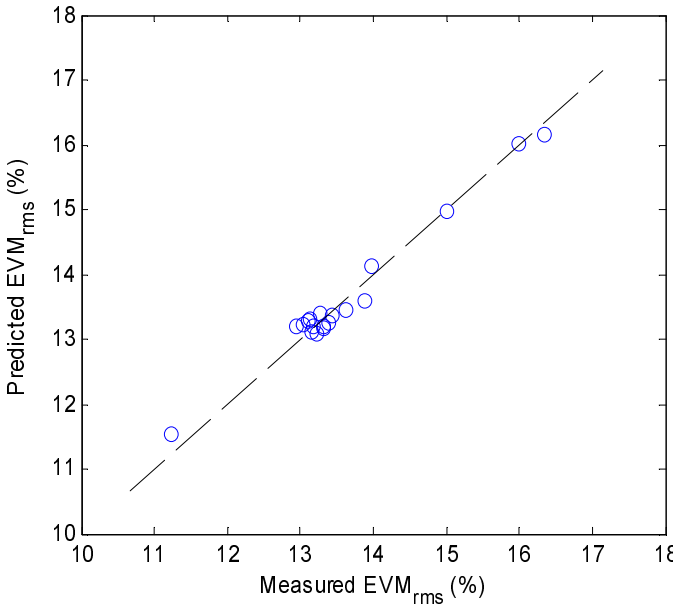

Figure 5.23. Specification tracking using alternate-test methodology: EVM.

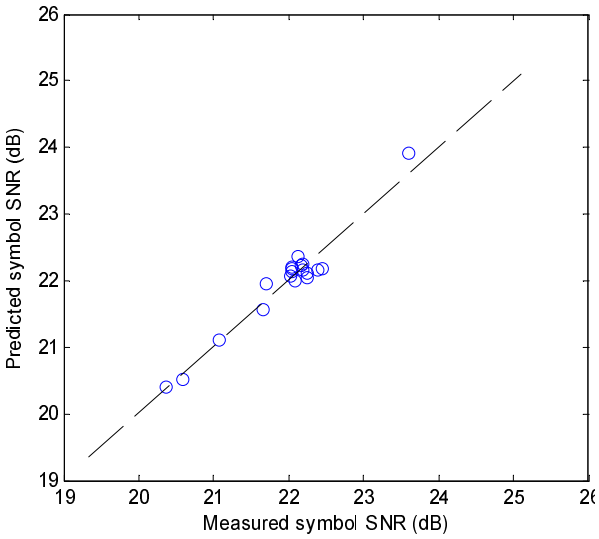

Figure 5.24. Specification tracking using alternate-test methodology: modulation-SNR.

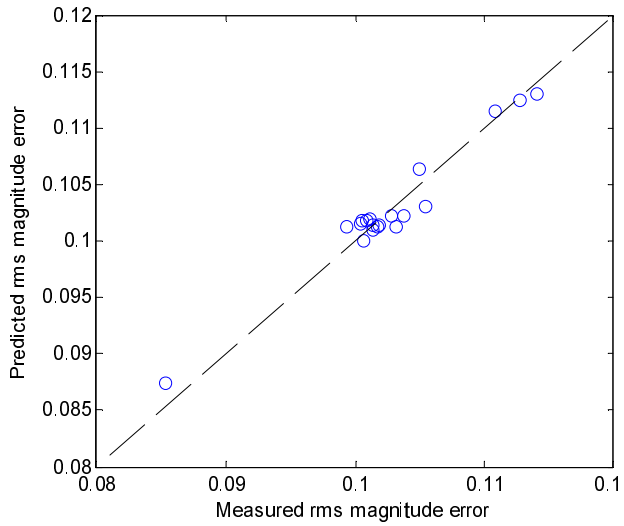

Figure 5.25. Specification tracking using alternate-test methodology: RMS magnitude error in symbol constellation.

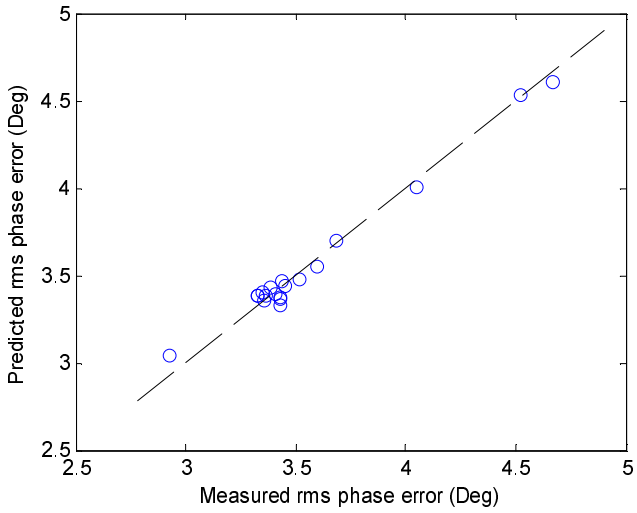

Figure 5.26. Specification tracking using alternate-test methodology: RMS phase error in symbol constellation.

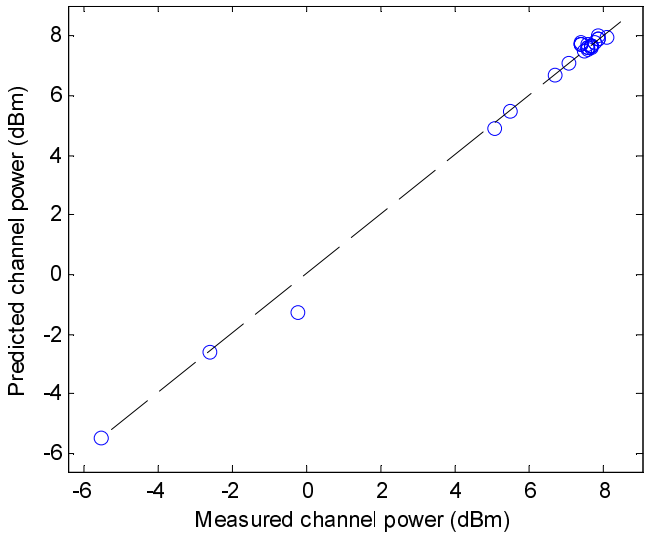

Figure 5.27. Specification tracking using alternate-test methodology: Channel-power.

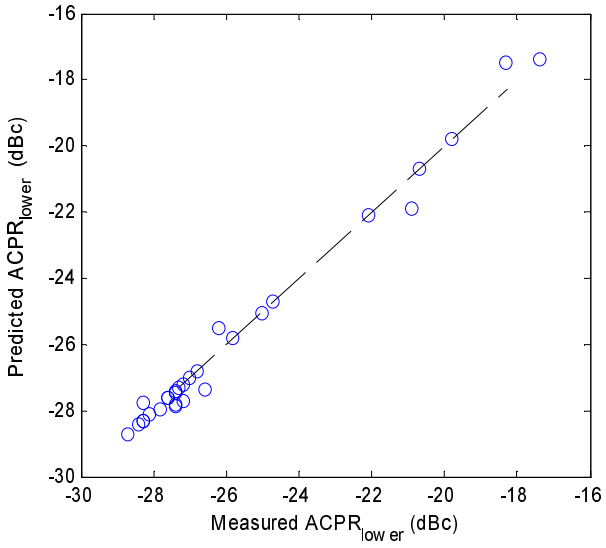

Figure 5.28. Specification tracking using alternate-test methodology: ACPR$_{lower}$.

Testing time considerations are shown in Table 5.1. For frequency-domain specifications, frequency sweeping time over the frequency span by the spectrum analyzer was used for test time estimate. For modulation-domain specifications, the time for baseband

signal processing and D/A interfacing for multiple data-frames was used for test time estimates. ACPR and channel power were measured using 10 frequency sweeps in max-hold mode using 1 kHz resolution bandwidth over 900 kHz frequency span centered around 1.575 GHz. 20 Frames, each having 600 symbols, was used to compute modulation-domain specifications. DSP (Matlab) processing [6] and DAQ card interface overhead occupies a considerable part of the test time. Conventional two-tone test was the fastest. It should be noted that, the timing values were in real-time delays without the test automation of a production testing ATE.

Table 5.2. Test time estimates.

Test setup	**Real time from start to end**
Two-tone test (gain, TOI)	< 1 sec
ACPR, channel power	~10 sec
Modulation-domain specs	>1 min
Alternate testing	~2 sec

Table 5.3 compares the prediction accuracy values obtained in alternate testing with that of conventional testing methodology for the RF test instrumentation ([12], [13]) used in the above experiment. It should be noted that the conventional specification measurement accuracy values for complex specifications, e.g. ACPR, EVM, are not specified in the instrumentation datasheet. For complex specifications, these accuracy values are derived from more fundamental instrumentation specifications, e.g. maximum amplitude error of a spectrum analyzer [12], maximum SNR in A/D or D/A [13]. For modulation-domain specifications, apart from the specification of the test instrumentation, the accuracy of phase-frequency detection of the digital-IF carrier in DSP affects the accuracy of the conventional specification testing. In Table 5.3, we assumed that the captured symbol magnitude-accuracy

is primarily determined by the SNR present in the noisy A/D card used as a part of the ATE. The input noise-floor for the A/D used was measured to be -65 dBm in 50-200 kHz frequency range. The accuracy of symbol phase-error is primarily determined by the phase-recovery uncertainty due the finite number of waveform-samples (40 samples) within every cycle (0-2π) of the 100 kHz digital-IF carrier, followed by the finer reduction (by a factor of 0.08-0.1) in phase-error obtained using the constellation rotation algorithm. The corresponding uncertainty (after constellation rotation) in the computed values of EVM and SNR represents the accuracy of EVM and SNR test in conventional testing method. Table 5.3 shows that there is little loss in specification test accuracy when using short and single alternate test instead of multiple and long conventional tests.

Table 5.3. Specification test accuracy comparison.

Specification	| Max. prediction error | in alternate testing	| Accuracy | of conventional testing
Gain	0.66 dB (Figure 5.21)	0.4 dB
TOI	0.48 dBm (Figure 5.22)	0.8 dBm
ACPR	0.83 dB (Figure 5.28)	0.8 dB
Channel power	1.10 dBm (Figure 5.27)	0.4 dB
EVM_{rms}	0.32 % (Figure 5.23)	0.28 %
Magnitude error	2.4e-3 (Figure 5.25)	2.81e-3
Phase error	0.11 deg (Figure 5.26)	0.9 deg
Modulation SNR	0.31 dB (Figure 5.24)	0.1 dB

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[13] National Instruments PCI 6111 Data Acquisition card datasheet, 2003.

CHAPTER 6

SYSTEM-LEVEL LOOP-BACK TESTING APPROACH FOR WIRELESS TRANSCEIVERS

In the previous two chapters, the proposed alternate test methodologies for wireless systems used external RF test instrumentation. The proposed approaches used RF signal generators to apply two-tone RF stimulus to perform specification test of the receiver. For testing the transmit system, the proposed approach uses an external spectrum analyzer to capture the spectral test response. In this chapter, a new loop-back approach using alternate testing has been described. The objective of the loop-back test is to eliminate the external RF instrumentation dependency.

6.1. Previous Work in Loop-back RF Testing

In this proposed loop-back technique, an optimized periodic bitstream is used to efficiently test the specifications of the transmit and the receive subsystems of the RF transceivers using the alternate test framework. In this framework, the test specifications of the circuit-under-test are measured using a specially crafted stimulus, which is applied to the circuit-under-test and the specification values are computed (predicted) from the observed test response [1]. In the proposed approach, an optimized periodic bitstream generated by the DSP and modulated by the transmit modulator at the baseband is used as the test stimulus. The output of the transmit subsystem to this stimulus is fed back into the receive subsystem

using minimal on-board hardware. The test response at the output of the receiver subsystem is processed by the DSP and the linear and the nonlinear specifications of the transmit and the receive subsystems are computed (predicted).

Unlike earlier reported transceiver test strategies ([2] - [4]), information about the specification values for the transmit subsystem are successfully decoupled from that for the receive subsystem and the specifications for both subsystems are computed using the looped-back baseband test response only. Hence, using this approach, expensive RF ATE instrumentation can be avoided and it addresses the specification test problem of RF subsystems in a tester independent architecture. Moreover, since a single bitstream sent from the baseband is used for the entire test, the overall test time for multiple specifications is reduced. Also, the issue of high simulation cost of RF subsystems is addressed by using behavioral models to simulate the RF subsystem-under-test for test generation. Behavioral model parameters are perturbed to generate different instances of the transceiver system, which are used for test generation, calibration, and validation of the test methodology.

In [3], the authors propose in a conceptual manner to use a dedicated down-conversion path on the same chip for down-conversion of the transmitter output back to baseband. At the same time, by the means of an RF coupler, it proposes to feed the transmitter output back into the receiver input. However, the concept presented has not been supported by experimental data in. In [2], the authors have proposed a loop back test strategy in which, the structure of the device-under-test (DUT) corresponds to a chain of building blocks (i.e. PA, mixer, LNA, band pass filters) connected in a loop. The authors of [2] propose to use a pseudo random test stimulus to measure the ACPR specification of the transceiver system. The response of the subsystem to this stimulus has a large number of frequency bins in the up-converted RF frequency spectrum. Therefore, measuring the power over such large number of tones requires long test times and expensive RF automated test equipments (ATEs).

In the past, alternate test methodology has been used in [5] to test individual RF modules using transient tests. In [6], authors have proposed a method to test RF transmitter specifications using optimized periodic bitstreams using a spectrum analyzer at the output of the RF transmitter. In [7], the authors attempt to test LNA and mixer of a receive subsystem for testing of the RF specifications. In the work presented in this chapter, a similar alternate test methodology is employed to reduce the test cost of such RF subsystems.

6.2. Alternate Testing using Loop-back Stimuli

As described in literature [1] and [5], the process variations affect both measurements and specifications directly. If one can get a measure of the variations in process parameters, then it is possible to compute the specification values directly. But, the information related to process statistics is not readily available. The other possibility is to compute the specifications from the measurements, eliminating the standard specification tests. Alternate test uses the latter approach and builds a correlation between the measurements and the specifications by selecting an optimal test stimulus. This enables alternate test to replace the standard specification test and speed up the whole procedure of specification testing by using the optimized test stimulus for obtaining the measurements.

Alternate tests use a specially crafted test stimulus, to calculate (predict) the specifications of the CUT from its response using nonlinear regression functions. To generate the nonlinear regression function, a set of training CUTs are selected from different production lots. The test stimulus is applied to each of these CUTs and their resulting test responses are sampled and stored. Simultaneously the output specifications of these devices are measured using the conventional specification test setups. The sampled transient

measurements are mapped onto the specifications of the device using nonlinear regression functions. During production test, the measured response of the CUT is mapped onto the specifications using these functions. A flow diagram of alternate test procedure is shown in Figure 6.1.

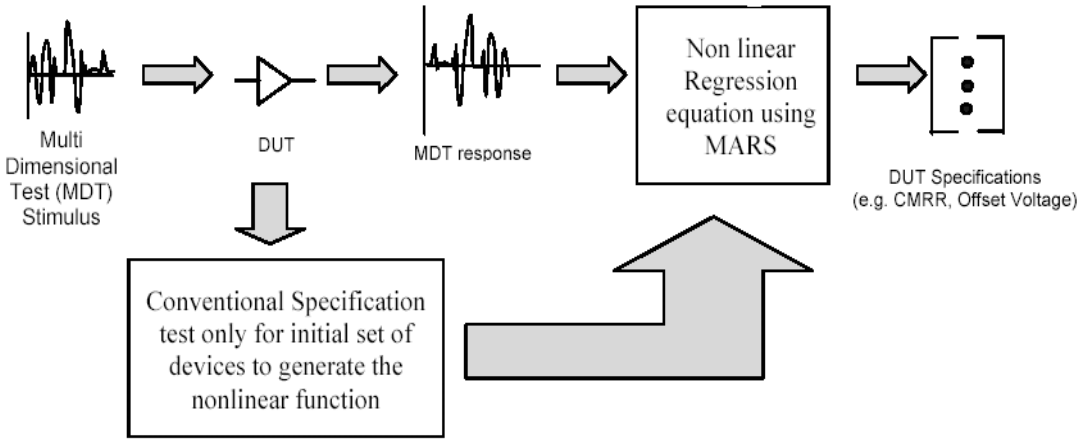


Figure 6.1. Alternate test framework used to predict DUT specifications.

Multivariate Adaptive Regression Splines (MARS) [8] is used to build the nonlinear regression functions. The MARS algorithm depends on the selection of a set of basis functions and a set of coefficient values corresponding to each basis function to construct the nonlinear regression model. The model can also be visualized as a weighted sum of basis functions from the set of basis functions that span all values of each of the independent variables. In this approach, the objectives of automated test selection in alternate test paradigm are:

1. to select an optimal bit sequence at the transmitter baseband as test stimulus,
2. to predict circuit specifications accurately from alternate test response.

6.3. Test Architecture and Test Approach

Figure 6.2 shows the proposed test architecture for testing transmit and receive subsystems. In the baseband, the DSP acts as a periodic bit sequence generator and the transmitted bits are modulated by the baseband modulator using the corresponding digital modulation scheme of the communication protocol, e.g. Gaussian minimum shift keying (GMSK) [9] for GSM transceivers. The modulated bit sequences are up-converted in frequency and amplified using the mixer and power amplifier of the transmit RF subsystem. The transmitted RF signal is fed back into the receive subsystem using on-board dedicated test hardware. The receive subsystem down-converts the RF signal into the receive baseband with addition of minimal amount of noise. The DSP, uses an A/D converter to capture the baseband receive data and performs alternate test based analysis on the spectral content of the data to predict target specifications of the transmit and receive subsystems.

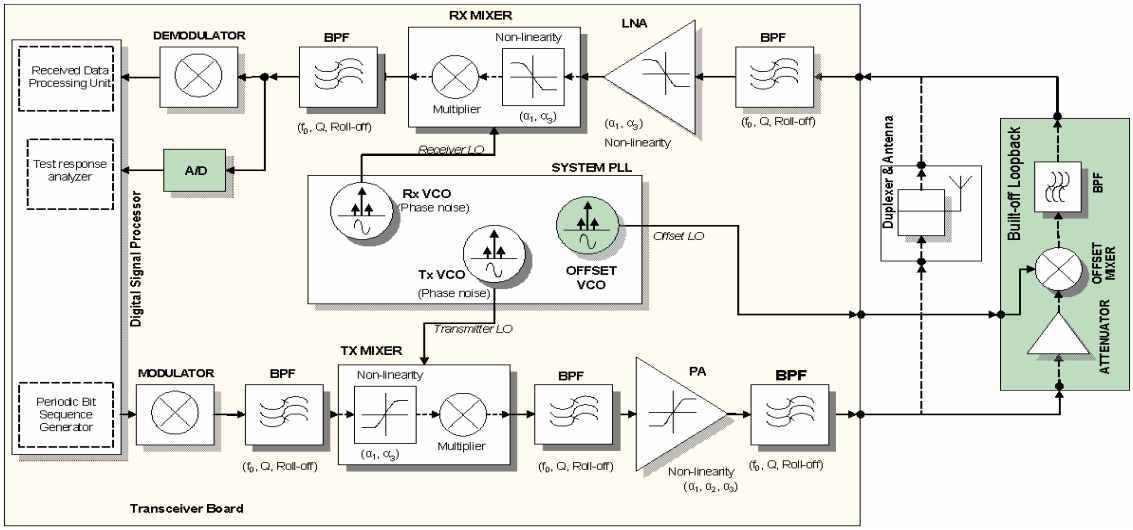


Figure 6.2. Test architecture for testing of the RF subsystems of a transceiver.

Inside the dedicated on-board test hardware, an attenuator is used to reduce the transmitted power level within the input dynamic range of the receive subsystem. An offset mixer and a band-pass filter are used to shift the frequency of the transmitted RF signal within the receive frequency band of receive subsystem. For this loop back scheme to work, the offset VCO, the offset mixer, the BPF, the attenuator and the baseband A/D (shown as shaded blocks in Figure 6.2) remain as additional hardware overhead, which obviate the RF ATE instrumentations used in conventional methods of measuring specifications. In this architecture, the duplexer and the antenna combination are not included in the system-under-test. In this work, the proposed scheme test scheme has been validated using a GSM RF transceiver as test vehicle.

6.4. Behavioral Modeling of the System

The test stimulus selection for the proposed test scheme uses behavioral level simulation of the subsystems under test. Although, the transistor-level simulations for all the sub-modules can yield high accuracy of simulation, the long simulation time makes this approach impractical. The larger the size of the process and circuit parameter space, the more the number of iterations for a deterministic test selection algorithm.

Moreover, the primary objective of test generation is to determine the optimal set of test stimuli ([6], [7]), rather than to verify the functionality of the design. Hence, as long as the behavioral approximations preserve the relative "goodness" of one possible test stimulus versus another, it can be used for fast test generation with little loss in test accuracy as shown in [6] and [7]. The underlying assumption is that the variations in specification data and

measurement data follow the same statistical trend under behavioral parameter perturbations as they would for transistor level parameter perturbations.

Since, in the proposed approach, the measurement space is selected to be the amplitude spectrum (i.e. amplitude vs. frequency) of the test responses observed at the baseband output of the RF subsystem-under-test, all the simulations for test generation are performed in the frequency domain. For an RF subsystem in a narrowband wireless RF transceiver architecture, amplifiers, filters, mixers, frequency synthesizers etc. are modeled by using an approach similar to that of [7] and are described below in brief:

Filter: The transfer function of the band-pass filters of the RF subsystem (e.g. band-select filter) are realized as linear transfer functions with different gains at different frequencies.

Amplifier: The amplifiers of the RF subsystem (e.g. LNA, PA) are realized by implementing a nonlinear transfer function of the type [10], $y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$. Where, α_0 = DC offset, α_1 = small signal gain, and α_2, α_3 = nonlinearity coefficients. These coefficients are used to realize the linear (gain) and nonlinear (harmonics and inter-modulation terms) effects of the amplifier. The time domain input-output nonlinear behavior is represented in frequency domain description as mapping of the sum of different input tones (in both magnitude and phase) to the corresponding output tones (magnitude and phase) [7].

Oscillator: The behavioral model of frequency synthesizer or oscillator is realized as a set of amplitude values [$X(f)$] corresponding to the different frequencies.

Mixer: For test generation purposes, the mixer of the RF subsystem is modeled as a nonlinear transfer function followed by an ideal multiplier. The nonlinear transfer function is realized in the same manner as is done for the amplifier. The frequency mixing operation is

realized by the multiplication operation [7], $y(t) = C\, x_1(t)\, x_2(t)$. The conversion gain and –1dB compression point are used to characterize the behavioral model of the mixer.

6.5. System-Level Test Generation

In the proposed approach, a random search based selection technique (as opposed to deterministic test generation algorithm based optimizer) is used to generate the required test bitstreams. The objective of the test selection procedure is to achieve prediction error in the mapping function (Section 6.2) lower than a given error threshold (input to the algorithm). The inputs to the algorithm are:

1. The data packet size of the communication protocol (N), which is dependent on transmit data-frame size and the baseband data rate.
2. An error vector which corresponds to acceptable error in prediction values of different transmit and receive sub system specifications (Δ_{ERR}).

The random search based test selection algorithm is as follows:

BEGIN

1. Input N and Δ_{ERR}
2. Select at random a new bit pattern of size N
3. Apply the candidate bit pattern to multiple transceiver instances (generated by perturbing its behavioral parameters) and capture the response at the base band of the receiver
4. In parallel, measure the specifications of the transmitter and receiver subsystems using conventional test set up
5. Compute nonlinear regression models (using MARS) from the captured baseband receiver spectrum onto the subsystem specifications
6. Apply the bitstreams to a different set of transceiver instances and predict the specifications using previously computed regression models
7. If for any specification, the maximum error in predicted specifications is greater than the corresponding threshold Δ_{ERR}, go to step 2
8. Set test stimulus := selected bit sequence

END

Using the above random search based test selection method, the most optimal stimulus is not guaranteed. Moreover, for significantly low Δ_{ERR} values, a unique test bit sequence may not exist. Ideally, it is desired to have a deterministic selection process for satisfying the Δ_{ERR} error thresholds for all specifications. However, any deterministic test stimulus search method using iterative optimization over continuous search parameters, such as gradient search technique used in [7], may not be used in this problem, since the test search space consists of discrete and discontinuous values (bit pattern). Other test ranking based

approaches proposed in [6] may be used to guarantee the selection of a near-optimal test stimulus. The objective of the algorithm presented above is solely to test for the existence of such bit sequences and to show the feasibility of loop-back test using these periodic bit patterns from baseband. These experimental results, first using behavioral simulation and then validating against hardware measurements, are presented in the following section.

6.6. Experimental Results

For the transceiver architecture described in Section 6.3, the proposed test approach has been validated using (1) behavioral simulation and (2) hardware setup.

6.6.1. Simulation Result

In this case, a baseband bit sequence modulated using 200 kHz baseband modulation carrier and MSK [9] modulation scheme is selected as test stimulus. The periodicity of baseband bit sequence is assumed to be 8, in this example. For system-level frequency domain simulation, the baseband spectrum was generated using fast-fourier-transform (FFT) of the MSK modulated data of transmitter. The RF front-end is designed for 900MHz GSM band. The system is simulated using the frequency-domain behavioral modeling approach described in Section 6.4. The spectrum obtained at the transmitter baseband, the transmitter output and the receiver baseband are shown below as examples.

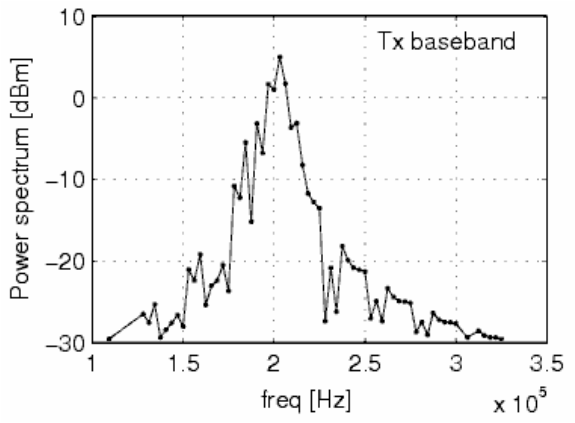
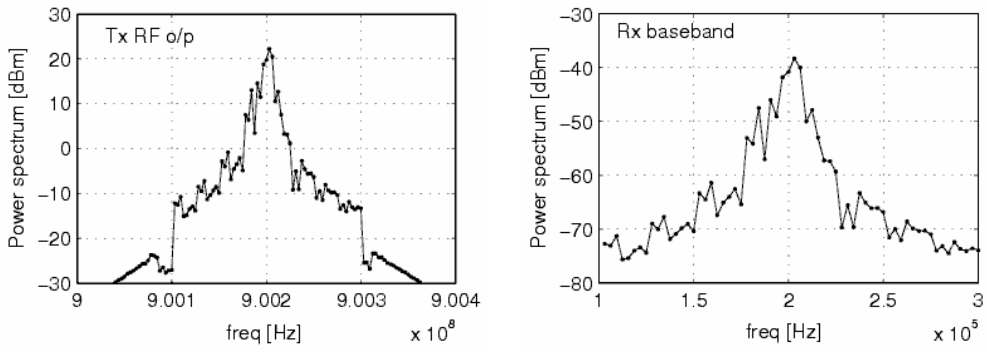


Figure 6.3. Transmitter baseband output.

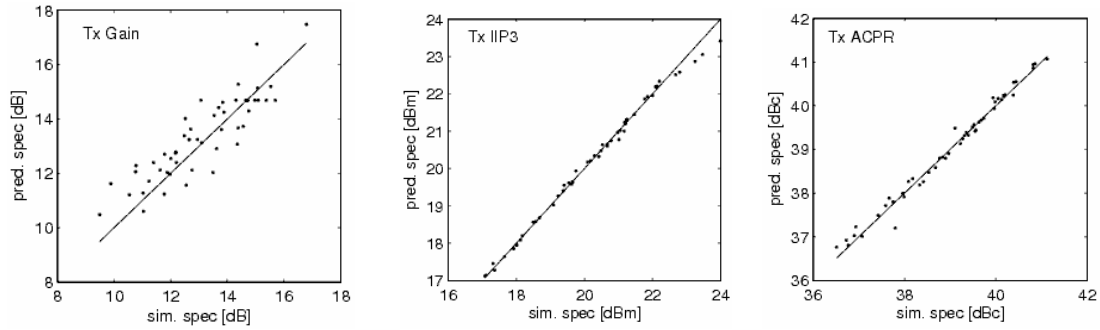


(i) (ii)

Figure 6.4. Spectrum at (i) transmitter RF output and (ii) the receiver baseband output.

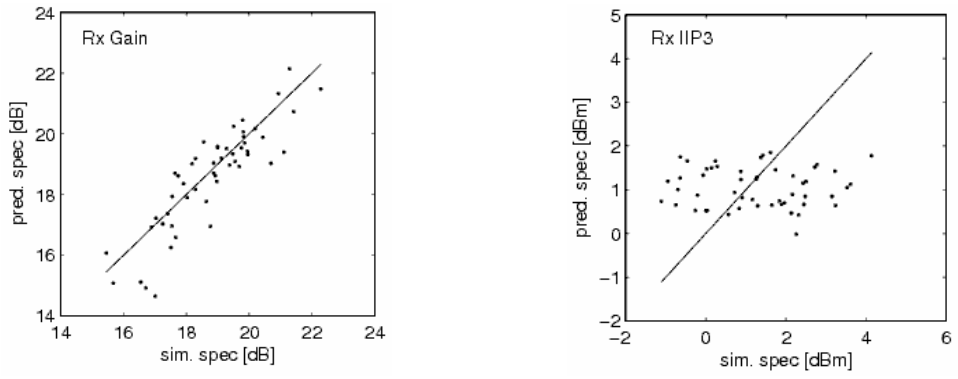
All behavioral parameters of transmit and receive subsystems are perturbed for creating different instances of the transceiver-under-test. A set of training instances are used for computing the nonlinear regression equation using MARS (Section 6.2). Another set of validation instances are used to validate the proposed method. The random search based test bit sequence selection (Section 6.5) is done and errors in specification prediction are evaluated. For an accurate specification prediction, the predicted specifications would track the simulated specification values.

The scatter plots of the predicted specifications vs. the simulated specifications are presented in Figure 6.5 and Figure 6.6. The closer the predicted specification values are located to the straight-line having slope +1 (representing error-free predictions), the higher the effectiveness of the test bit sequence. In the experiments performed, it is observed that transmit subsystem specifications are predicted with much less error than the receive subsystem specifications. In particular, prediction errors for IIP3 of receive subsystem are high, because the highly nonlinear behavior of the receive subsystem (represented by a poor nominal IIP3 value) is not effectively captured by the regression equations used in specification prediction. In the presented scatter plots, one of the multiple candidate patterns is used, which shows the feasibility of using periodic bit sequences for the proposed loopback test architecture for RF transceivers. However, the bit sequence corresponding to the lowest prediction error may be omitted in this random search based test selection algorithm.



(i) (ii) (iii)

Figure 6.5. Tracking of transmit subsystem specifications: (i) Tx gain, (ii) Tx IIP3, (iii) Tx ACPR.



(i) (ii)

Figure 6.6. Tracking of transmit and receive subsystem specifications: (i) Rx gain, (ii) Rx IIP3.

6.6.2. Measurement Result

The proposed test generation methodology was also validated using hardware measurements. In this case study, the transmission system used GMSK [9] modulation scheme with BT = 0.3 at the base band. The GMSK modulated bit sequence of size equivalent to GSM TCH/FS [11] data-frame was used as test stimulus. Channel bandwidth of 200 kHz and RF carrier frequency of 900MHz were used. Matlab software interfacing with a 5 MSamples/sec DAQ card was used to emulate baseband DSP. Filters, LNA, PA, mixers, antenna were designed on PCBs using off-the-shelf components.

In the validation steps, at first, different modules (e.g. LNA, PA, filters, mixers) constituting the transceiver were characterized individually. Different components and their corresponding characterization data are presented in Table 6.1. Figure 6.8 and Figure 6.9 show the characteristics of the different modules that constitute the wireless transceiver.

Table 6.1. Module characterization on hardware.

	Gain (dB)	P-1dB (dBm)	IIP3 (dBm)
Transmit Mixer	-33	2.8	15.9
Transmit Amplifier	13	3.5	16.5
Receive LNA	10	-5.1	4.6
Receive Mixer	5.8	-5.2	11
Band Pass Filter	-2.7	--	--

From the characterization data obtained, the coefficients describing the input-output nonlinear (LNA, PA, mixer) and linear (filters) modules were computed and then used as the behavioral component parameters of the test architecture described in Section 6.4. Using system-level frequency domain behavioral simulation, test generation was performed (Section 6.5) and a bitstream was selected as test stimulus.

Next, transmit and receive chains were characterized separately. This step is only essential for validation of the proposed test method against a set of known measurement data and is not required for performing production test based on the proposed method. As per the characterization data, the transceiver loop was initially tested by transmitting a single tone (900.2 MHz, -16dBm) from the baseband signal generator. The received baseband spectrum is shown in Figure 6.9(ii). From the figure and the values presented in Table 6.1, the channel attenuation was found to be approximately -38dB.

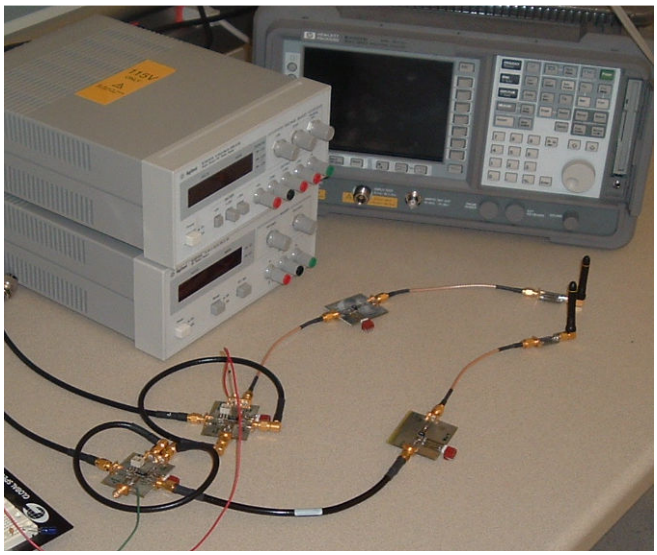
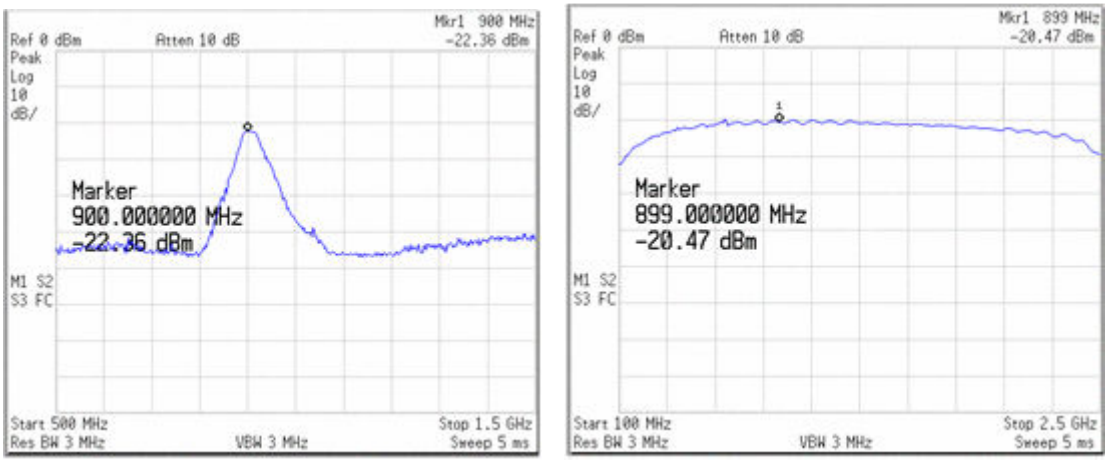


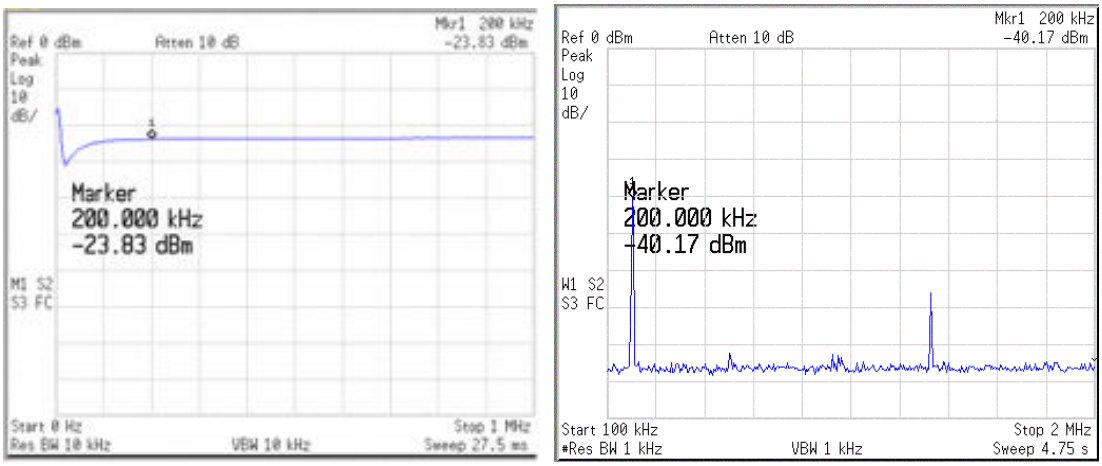
Figure 6.7. Loopback test measurement setup.

After the characterization of the modules and the system were complete, the entire transceiver system is connected in loop-back mode and spectral purity of the data acquisition card was analyzed and calibrated. Figure 6.10(i) shows the captured waveform using the National Instruments (NI) data acquisition card.. The spectrum of the acquired data is shown in Figure 6.10(ii). The 0-200 KHz channel in the left half figure is enlarged and shown in the right half of Figure 6.10(ii). (In figure, the amplitudes of the spectral components were not normalized by the sample size before converting to decibels).



(i) (ii)

Figure 6.8. Module characterization: (i) BPF (-20 dBm input) (ii) LNA (-30 dBm input).

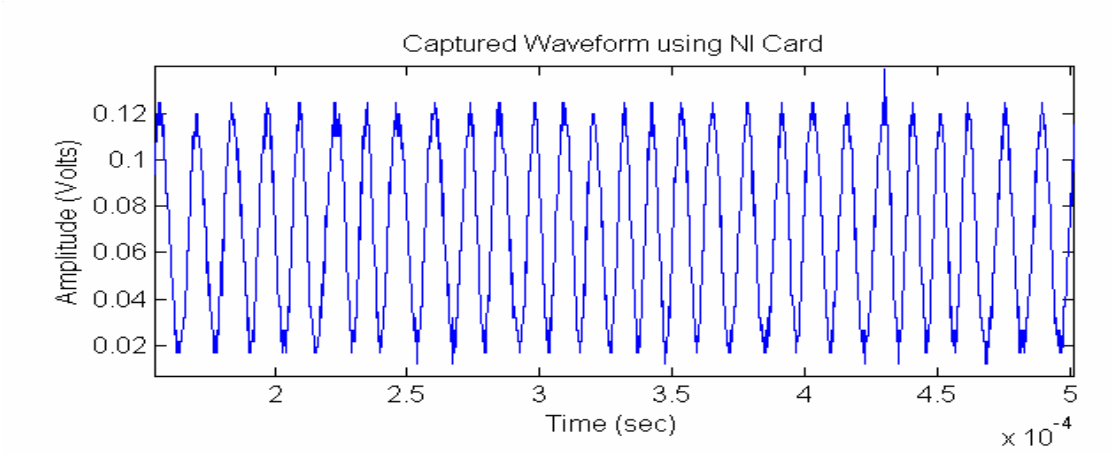


(i) (ii)

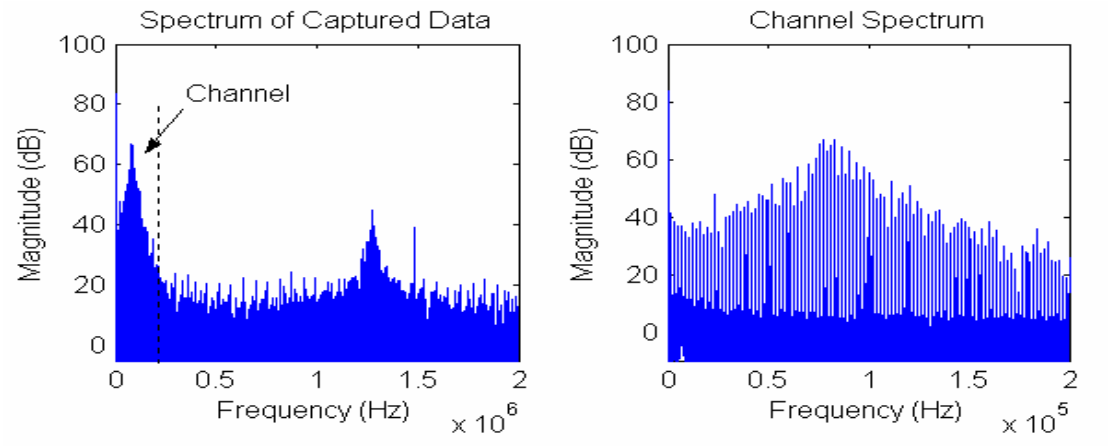
Figure 6.9. Module characterization data: (i) receiver mixer conversion gain (-30 dBm i/p) (ii) receiver mixer nonlinearity.

Next, the test stimulus obtained from behavioral simulation based test generation was applied from the transmitter baseband and received loop-back test response waveform is captured.

During the test generation, the nonlinear regression model using MARS was computed from the behavioral simulations (explained in Section 6.2). Using the regression models and the captured test response spectrum from hardware, individual transmit and receive subsystem specifications were predicted. The predicted specifications and the corresponding measured specifications are presented in Table 6.2.



(i)



(ii)

Figure 6.10. (i) Modulated waveform captured in DAQ card (ii) corresponding spectrum.

Table 6.2. Predicted specs using hardware data.

	(1) Actual specification	(2) Predicted specification
RX Gain	20 dB	19.0 dB
RX IIP3	-1.26 dBm	0.8 dBm
TX Gain	-1.6 dB	-3.3 dB
TX IIP3	15.9 dBm	20.3 dBm

In the experimental setup, the predicted specifications closely follow the actual specifications (measured using conventional measurement methods). For go/no-go test, the deviation of the predicted values from the actual specification values may (or may not) be tolerable and will depend on the specification test limits. The key differences between these two methods are:

Conventional test in (1) uses:	Alternate loop-back test in (2) uses:
• single-tone and two-tone stimuli • RF measurements at transmitter & receiver o/ps • RF signal source and spectrum analyzer	• baseband transmitter data as test stimulus • baseband loopback spectrum for spec. prediction • loopback hardware and no RF instrumentation

Hence, using the proposed loop-back alternate test approach for wireless transceivers would result in removal of expensive RF test instrumentation and RF test response capture complexity. Moreover, it would introduce the possibility of performing entire system-level test in an ATE independent manner using autonomous built-in test performed from baseband.

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APPENDIX A

DEVICE INTERFACE BOARD DIAGNOSTIC TECHNIQUE USING STRAY CAPACITANCE MEASUREMENT

Parasitics play an important role not only in design but also in test and diagnostics of circuits. In ATE hardware setup, the accuracy, repeatability and testing time are affected by the parasitics present in the ATE hardware design. In this chapter, an automated fault diagnostic method for the device interface boards is described.

A.1. Stray Capacitance on Device Interface Boards

During the testing of a device, test stimuli are applied to the device-under-test (DUT) using test hardware and software. Then the DUT response is measured and analyzed to determine if the DUT is operating according to its specifications. The test hardware includes the load-board or device-interface-board (DIB), probe-card, connecting cables, socket, signal generating instruments and measuring instruments. In automatic testing equipment (ATE), the test hardware can be controlled by the test software which is often written in a high level language such as C or Pascal. Depending on the test method, the parasitics, such as stray capacitance, inductance, resistance, etc., associated with the test hardware can affect the test stimulus and/or the test response. In general, the parasitics of test hardware are intended to be minimized or compensated by efficient design and

assembly of the test hardware [1]. Good test techniques [2] that cancel the effect of parasitics on the test results may also be used to address the problems posed by the parasitics. However, the test stimuli and response signals are seldom free from the parasitic effects. If these effects are not taken into consideration in the test response analysis, a faulty circuit can potentially be classified as a good circuit and/or vice versa, resulting in poor fault coverage and/or poor yield coverage respectively. Therefore, accurate estimation ([3], [4]) and measurement ([3], [5]) of parasitics are necessary to improve the performance of the tests.

In this chapter, a simple technique for making accurate and precise measurement of parasitic capacitance on test hardware has been presented. This technique can be applied to measure the stray capacitance of different test hardware components, such as DIB interconnects, sockets, etc. The measured capacitance values can be used instead of the less accurate estimates obtained from the CAD tools or the specification data provided by the test hardware manufacturer. The proposed technique uses only a single port for performing measurements. Therefore, it can be used to detect shorts and opens of the DIB interconnects, switching faults in the relays, etc. without adding any extra circuitry on the DIBs. Experiments performed on Teradyne mixed-signal ATE ([6], [7]) showed that the stray capacitances can be measured with up to 1.5 pF of precision using the proposed technique.

A.2. Motivation

In this section the need of measuring the stray capacitance on test hardware instead of using other indirect and alternative methods of extracting parasitic capacitance is explained. The specifications of the input/output capacitance of different test instruments provided by the manufacturer can be used to get the respective worst-case values of stray capacitive loading. The CAD tools, which use the electrical modeling of the components, can be used to estimate the stray capacitance associated with the different test hardware units. However, specification data is usually more conservative; therefore, less accurate. On the other hand, the CAD based estimation schemes for stray capacitance fall short of the accuracy after a hardware component is fabricated. A prior estimate of the stray capacitance does not contain any information of the random variation in it, which is observed only after the hardware component is fabricated. Also, estimation may not detect any change in the parasitics because of the change in operating conditions, the aging, etc. A measurement can potentially give the exact value of the stray capacitance. Measurements can be performed periodically to track the value of the parasitics with the changing operating condition, or just to flag an alarm when it unexpectedly changes due to some test hardware fault.

A.3. Theoretical Analysis

Stray impedance of different test hardware components may be measured using any combination of DC, AC and transient measurement schemes. However, these

components, as illustrated in the case of a DIB interconnect in Figure A.1, often appear as a single-port network to the ATE and they may have no termination or a DC path to the ground. Therefore, the DC measurements as well as the AC measurements using different steady-state sinusoids can not be used to measure the electrical parameters of these components.

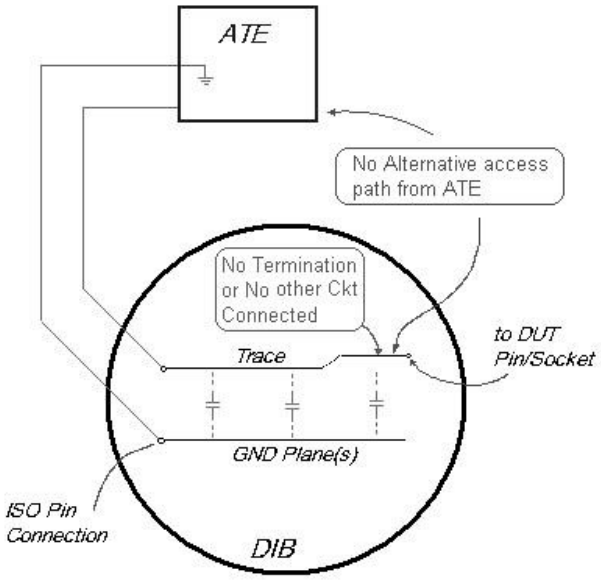

Figure A.1. Measurement criteria

The only way to measure the electrical parameters of these components is to excite them through the single access point available to the ATE and observe the electrical quantities (voltage and/or current) at the same access point over different time instants. Electrical charging/discharging characteristics and time-domain-reflectometry (TDR) use this transient scheme for measuring electrical parameters of these components. In this chapter, focus is only on the transient charging and discharging behavior of different components of tester hardware for measuring the stray capacitance associated with them.

The stray capacitance associated with a component can be charged (or discharged) from a voltage level v_1 to another level v_2 over a duration of t_1 to t_2 using a current $i(t)$ forced by the ATE. The amount of charge transferred to the stray capacitance is given by Equation (A.1) and the average stray capacitance value is given by Equation (A.2). For the given values of v_1 and v_2, the stray capacitance can be calculated, if the amount of charge transferred to the capacitor for changing the voltage from v_1 to v_2 is measurable. It is difficult to measure this charge using any practical instrumentation when it is in the general integral form as in Equation (A.1). However, if a region on the charging (or discharging) curve is selected such that the current forced by the ATE is fairly constant over that region, i.e., $i(t) = I$ for $v_1 \leq v(t) \leq v_2$, then the same can be measured with less difficulty (Figure A.2) and Equation (A.2) simplifies to Equation (A.3).

$$Q = \int_{t_1}^{t_2} i(t)\,dt \qquad \textbf{(A.1)}$$

$$C = \frac{Q}{v_2 - v_1} \qquad \textbf{(A.2)}$$

$$C = I\,\frac{t_2 - t_1}{v_2 - v_1} = \frac{I.\Delta T}{v_2 - v_1} \qquad \textbf{(A.3)}$$

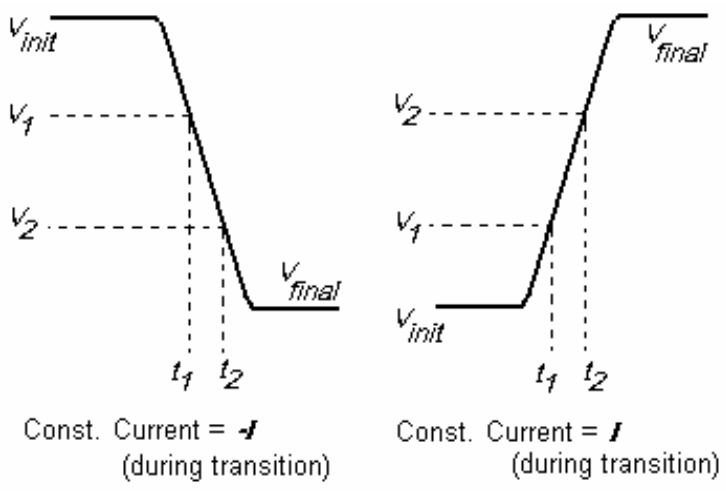

Figure A.2. Measurement technique

Theoretically, the values of v_1, v_2, and I can be selected by minimizing the first-order fractional error in the capacitance measurement appearing in the Equation (A.4). This will lead to the maximum possible accuracy and precision of the measurement. In practice, the availability, the range of operation, and the non-ideal behavior of the current/voltage sources, and the time measurement sub-system in the ATEs restrict the selection of these parameters.

$$\frac{\Delta C}{C} = \pm \frac{\Delta I}{I} \pm \frac{\Delta t_2 - \Delta t_1}{t_2 - t_1} \mp \frac{\Delta v_2 - \Delta v_1}{v_2 - v_1} \qquad \textbf{(A.4)}$$

A.4. Experimental Setup

In this section, an experimental setup (Figure A.3) for measuring stray capacitance of the interconnects of a DIB is described. The setup is used for testing a class of devices on Teradyne A580 mixed signal testers. This setup can be used for measuring stray

capacitance of other test hardware components, e.g., test sockets, connectors, etc., with little or no modification.

The setup uses the Per-pin Parametric Measurement Unit (PPMU) of the Teradyne A580 ATE [6] for forcing a constant DC current to the stray capacitance. The Time Measurement Subsystem (TMS) of the ATE is used for measuring charging/discharging time. Figure A.3 shows how the PPMU and TMS are connected to the tester signal path through software controlled relays. The procedure for measuring the stray capacitance in the signal path can be summarized as follows:

1. Close the relays to connect the TMS and the PPMU to the electrical signal path.
2. Program the PPMU to force an initial voltage V_{init} to pre-charge the stray capacitance in the signal path.
3. Program the TMS to trigger at two different threshold voltage levels, v_1 and v_2, for measuring the time difference of a changing voltage crossing these two threshold levels.
4. Program the PPMU to force a constant current to charge (or discharge) the entire signal path to a voltage level V_{final} sweeping past v_1 and v_2.
5. Measure the time ΔT between the events triggered in TMS while crossing the thresholds v_1 and v_2.
6. Calculate the total stray capacitance by substituting I, v_1, v_2, and ΔT ($= t_2 - t_1$) in Equation (A.3).

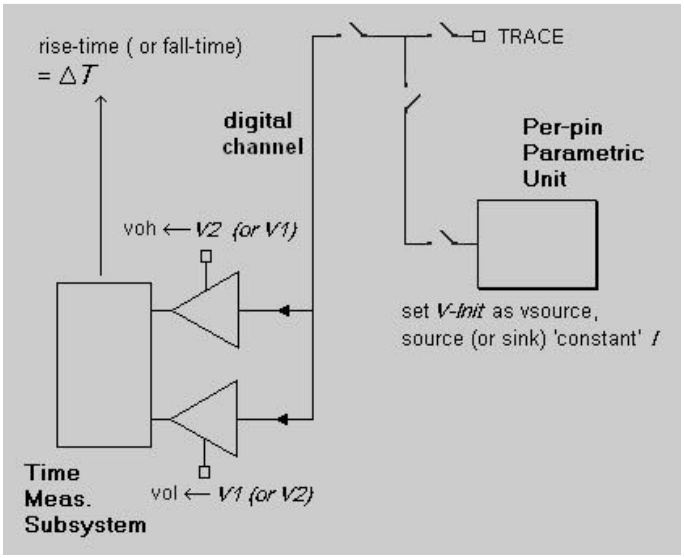

Figure A.3. Measurement Setup

If the above procedure is performed with the DIB board placed on the ATE (Figure A.4), the measured capacitance, $C_{w/B,}$ will include desired DIB trace capacitance along with the stray capacitances of the tester instruments and the electrical cables If the procedure is performed without the DIB, the capacitance measured, $C_{w/oB,}$ will include the stray capacitances of the tester instruments and the connecting cables only. Therefore, the DIB trace capacitance can be calculated using the procedure outlined below:

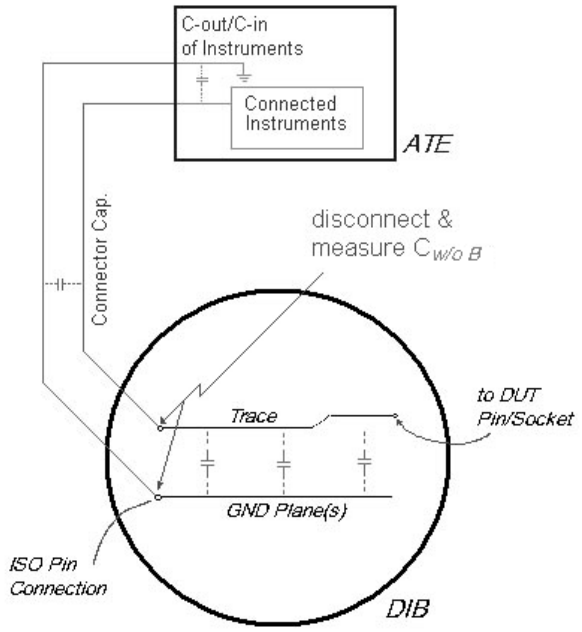

Figure A.4. Capacitive loading of the ATE

The time, $\Delta T_{w/oB}$, between the two events triggered in TMS without the board placed on the test-head is measured and the stray capacitance, $C_{w/oB}$, of the electrical path up to the test-head of the ATE is calculated:

$$C_{w/oB} = I.\Delta T_{w/oB} / (v_2 - v_1) \qquad \textbf{(A.5)}$$

The above procedure is repeated after placing the board on the test-head of the ATE. The charging (or discharging) time, $\Delta T_{w/B}$, and the stray capacitance, $C_{w/B}$, for the entire electrical path beginning from the ATE and ending at the DUT socket-pin is measured (Figure A.5).

The capacitance of the trace on the PCB is then computed as:

$$C_{Trace} = C_{w/B} - C_{w/oB} = I(\Delta T_{w/B} - \Delta T_{w/oB})/(v_2 - v_1) \quad \textbf{(A.6)}$$

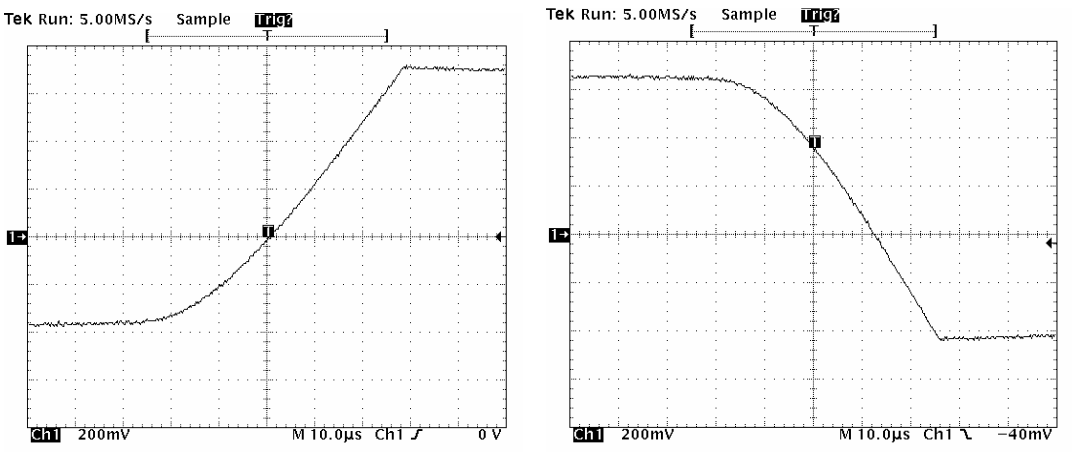

Figure A.5. Charging and discharging characteristics of the stray cap. with the DIB placed on ATE test-head (I = 80µA)

Similar procedure can be used to measure the stray capacitance of other test hardware components. For example, the capacitance of the electrical path after a relay can be calculated by taking the difference between the stray capacitances measured with the relay closed and the relay open.

A.5. Non-Idealities

The above procedure might ideally be used for any selected values of the parameters v_1, v_2, and I. These parameters might be selected based on the minimum and the maximum current/voltage handling capacity of the current source of the ATE, the test hardware and the minimum resolution of the time measurement sub-system of the ATE.

However, the experimental result revealed non-ideal behavior of the instruments that were used in the measurement setup. These non-idealities severely restricted the selection of the above parameters.

Initial measurement exhibited the presence of a leakage current, typically of the order of 10-15 μA, in the current/voltage source (PPMU) used in the measurement setup. Since the leakage current may vary across different ATEs, the measurement of the stray capacitance of a hardware component would suffer from poor repeatability across different testers unless the effect of this leakage is canceled. It can be shown that, if the leakage current is the same and remains constant during both charging and discharging of the stray capacitance, the error due to the leakage current can be completely corrected by taking the harmonic mean of the measured rise-time, t_{rise}, and fall-time, t_{fall}, as shown below:

$$\Delta T_x = 2\left(\frac{1}{t_{rise,x}} + \frac{1}{t_{fall,x}}\right)^{-1} \qquad \textbf{(A.7)}$$

In practice, the programmed current value should be selected as high as possible to minimize the relative effect of any leakage current on the measurement.

However, when the DC current source of the ATE is programmed to sink (or source) a higher current, the current takes longer time to reach the programmed current value. Figure A.6 illustrates the above phenomenon by showing the approximate slope ($\Delta v/\Delta t$) of the charging characteristics over the different voltages of the charging characteristics. The data for the graph is obtained by performing multiple charge transfer and measurement operations. In each of them, the (v_2-v_1) is kept small and the time-measurement sub-system is made to trigger and measure the Δt's at a different pair of

threshold voltages. Figure A.6 shows that the actual current approaches the programmed current value only toward the end of the charging (or discharging) characteristics. Therefore, both the threshold voltages need to be selected toward the end of the characteristics, which, in effect, also requires a small value of (v_2-v_1). However, a very small value of (v_2-v_1) causes the precision of the measurement to degrade, which is explained by the increase in the 3rd error term in Equation (A.3). Also, a very high value of the programmed current results in an overestimated measurement of the stray capacitance, because the value of the actual current during the charge transfer always remains less than the programmed value. Therefore, the selection of programming current for the current source and the threshold voltages for the time measurement sub-system are trade-offs between several mutually opposing requirements caused by the non-idealities in the measuring instruments.

The experimental result (Figure A.7), shows that a value of 180-200 μA for the current and a value of 0.5-1.0 V for the (v_2-v_1) with both v_1 and v_2 selected toward the end of charging and discharging characteristics, yield the best accuracy and precision for the measurement of extremely low capacitance using the PPMU and the TMS.

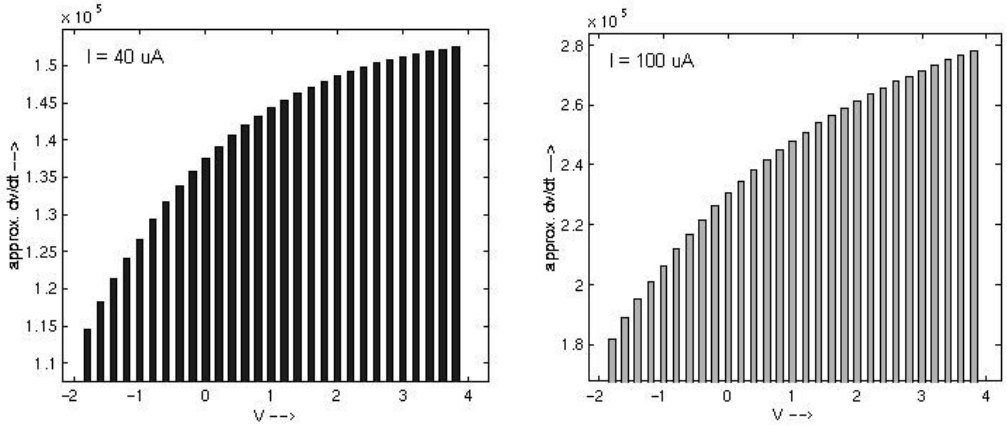

Figure A.6. Approximate slope of the charging characteristics for smaller and larger current

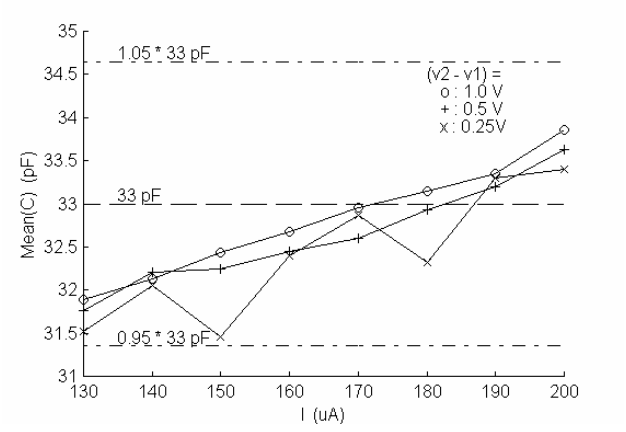

Figure A.7. Measurement of (33±5%) lumped capacitance for different values of *I* and ($v_2 - v_1$)

A.6. Measurement Results

In this section some case studies are presented in which capacitance of different ranges, including that of standard lumped capacitors, stray capacitance of the interconnects of test PCB, and test socket, are measured on Teradyne ATE platforms.

A.6.1. Experimental Validation Using Lumped Capacitors

Figure A.8(a,b,c) show three examples of measuring small capacitance values of the standard lumped capacitors using the proposed measuring technique. The accuracy and the precision of the measurements are well within ±0.5pF and ±1pF respectively.

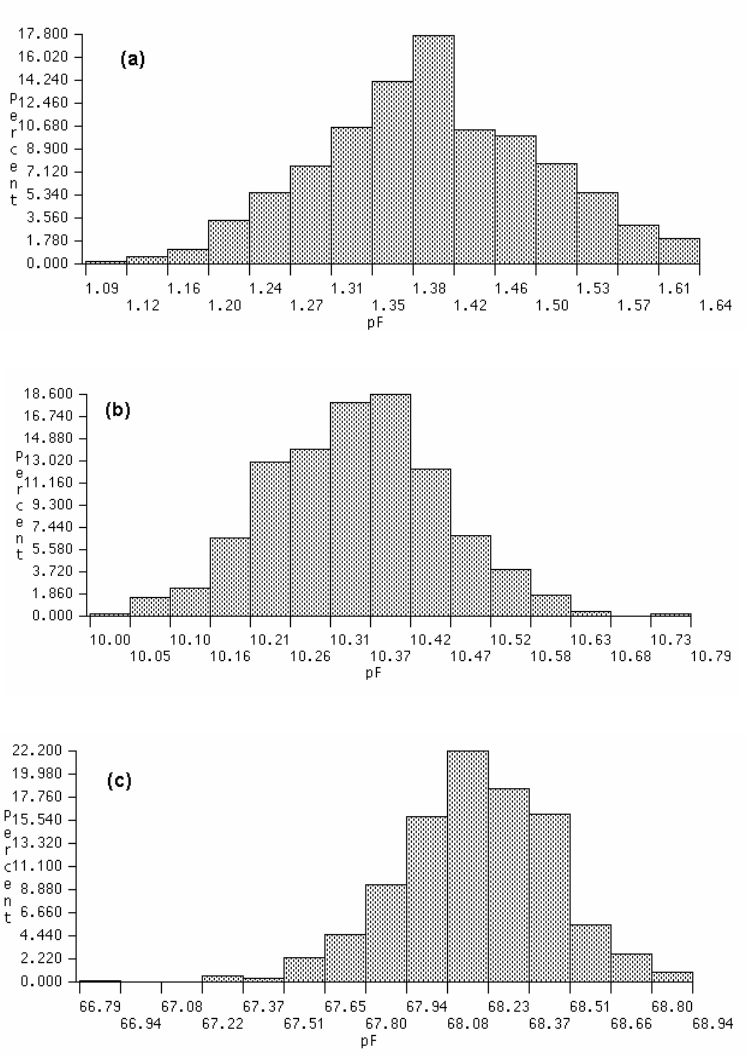

Figure A.8 Histogram of 500 measurements for standard lumped capacitors: I = 200μA, (v_2-v_1) = 1.0V; (a) 1±0.25 pF (b) 10±5% pF (c) 68±5% pF

A.6.2. Measurement of DIB Trace Capacitances

Several traces of two different signal planes of a DIB with varying copper-area are selected for measurement. If the fringing effect and the cross-coupling capacitance between adjacent traces are small [1], the capacitance of a trace with Cu-area A_{Cu}, lying within two GND planes separated by dielectric of t_1 and t_2 thickness and dielectric constant of ε_r, is given by,

$$C_{trace} = \varepsilon_0 \varepsilon_r A_{Cu} \left(\frac{1}{t_1} + \frac{1}{t_2}\right) \quad \textbf{(A.8)}$$

With accurate measurements, the measured C_{trace} values for different traces in a given signal plane of the PCB vary linearly with the corresponding values of the A_{Cu} (Figure A.9a) having a constant slope of C_{trace}/A_{Cu} (Table A.1). Moreover, for the traces in a given signal plane with equal copper-area, the values of C_{trace} are equal (Table A.1).

Table A.1. Measurement of the stray capacitance of different traces of two signal planes

Trace #	PCB plane	Cap. of trace pF	Cu-Area of trace cm^2	Cap. / Cu-Area pF / cm^2
1	*INT2*	17.21	0.25	68.84
2		30.40	0.43	70.70
3		39.59	0.57	69.46
4	*INT4*	44.70	0.66	67.73
5		44.94	0.67	67.07
6		45.88	0.68	67.47
7		46.04	0.68	67.71

However, the absolute value of accuracy for the above measurements can not be obtained since the standard values of the stray capacitances, unlike the capacitance values of the standard lumped capacitors, are not known for the PCB traces. However, the least-square-error w.r.t. the best-fit straight line through the measured values of the capacitance gives an estimate of the best possible accuracy. The absolute value of accuracy is equal to or greater or worse than the least-square-error of ±0.8pF (Figure A.9b). The precision of the measured stray capacitance of the PCB traces lies within ±1.5pF (Figure A.10a-c). The measurement of the stray capacitance is repeatable across the different Teradyne A580 mixed signal testers within the range of 1.5pF (Figure A.11a,b).

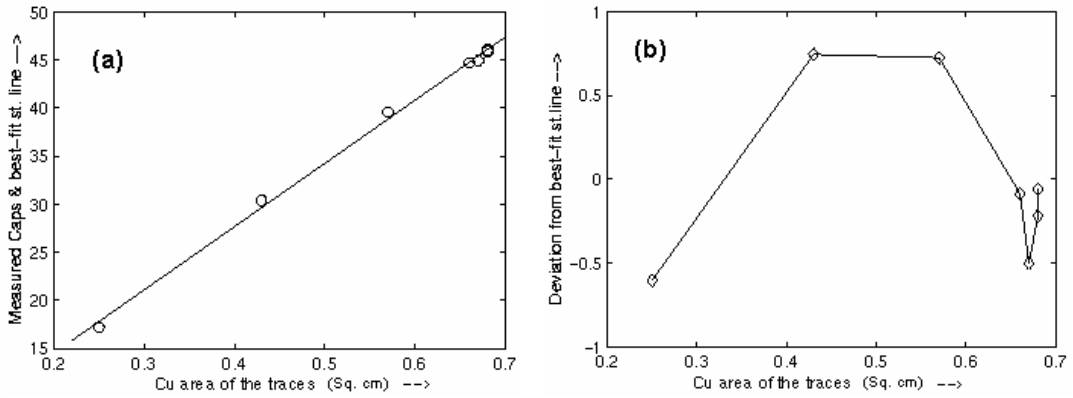

Figure A.9. Measurement accuracy: (a) Capacitance (b) Least square error vs. Cu-area

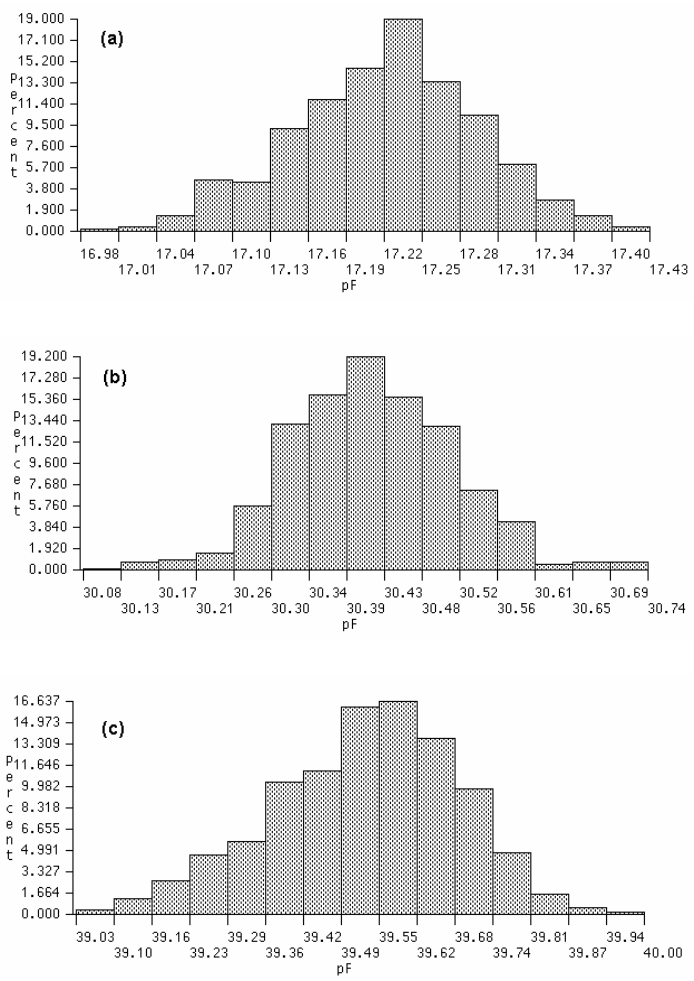

Figure A.10. Histogram of measurements for PCB traces of different Cu-areas: I = 190 μA, (v_2-v_1) = 1.0V; (a) 0.25cm^2 (b) 0.43cm^2 (c) 0.57cm^2

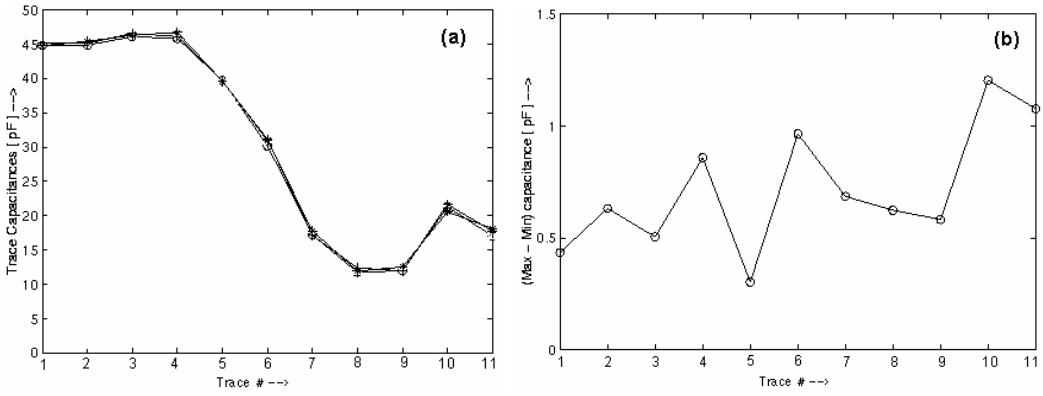

Figure A.11. Repeatability of the measurement of trace capacitances across five different ATEs: (a) Measured capacitances (b) The range (max.-min.) of deviation in the measured capacitances

A.6.3. Measurement of Stray Capacitance of Socket

In another case study, the stray capacitance of the pins of a micro-BGA test socket is measured on Teradyne's Catalyst mixed-signal ATE [7]. Since this capacitance in the DUT socket is extremely small and is located furthest away from the ATE, it is the worst possible case of measuring stray capacitance out of all the case studies presented. Initially, the stray capacitance of the traces reaching up to the socket pins and that of the pins are measured. The socket is then taken out of the test board and the stray capacitance of only the trace is measured (Figure A.12) and subtracted from the earlier measurement in order to calculate the stray capacitance of the socket pins alone (Table A.2).

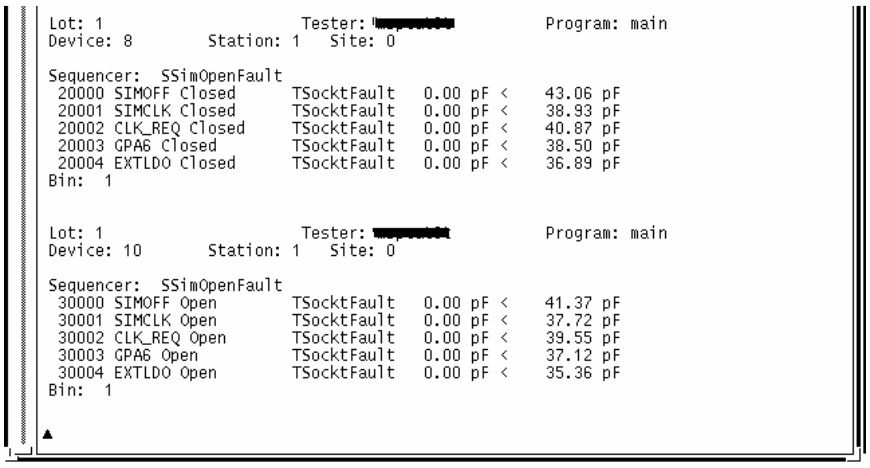

Figure A.12. Measurement of the capacitive loading of a test socket

Table A.2. Measurement of the stray capacitance of the socket pins of a micro-BGA test socket

Socket pin #	Cap. of the traces w/o socket (1) pF	Cap. of the traces with socket (2) pF	Cap. of the socket pin, (2) – (1) pF
1	41.37	43.06	1.69
2	37.72	38.93	1.21
3	39.55	40.87	1.32
4	37.12	38.50	1.38
5	35.36	36.89	1.53

A.7. Applications

The above capacitance measuring technique can be used on the ATEs for improving the performance of the test and the diagnosis of devices in several different ways. As demonstrated in the previous section, this technique can be applied to measure the

capacitive loading of the hardware components on a tester platform. If the specification of the capacitive loading for some hardware component is not available, and/or getting an accurate estimate of the same using the CAD tools is not practical, measurement of the stray capacitance is the only way to extract the parasitic loading information.

The measurement taken using this technique can be used for high-frequency testing, in particular, to adjust the test stimulus, and to adapt the test response analysis in order to cancel the effect of stray capacitive loading. The same can also be used to find whether an existing design of the test-board needs to be improved in order to reduce the capacitive loading on the critical test-signal paths.

The technique can be used for detecting shorts/opens on the electrical paths on the test board as demonstrated earlier in ([8], [9]) for detecting these faults for the interconnects in multi-chip-modules (MCMs). If the measured parasitic capacitance value is smaller than the expected capacitance value, the electrical path may contain an open-circuit in between. Similarly, a larger value measured capacitance indicates that the electrical path may be shorted to another. The value of the 'expected' capacitance required for this method can be obtained from the theoretically estimated value and/or the measurement made on other good, identical components of the test hardware.

The proposed technique can also be applied to test the proper switching action of the relays if the difference in capacitive loading of the two switched electrical paths is much larger than the precision of the measurement technique. In the following case study how the above technique is applied for testing the switching fault in three different relays (Figure A.13) is demonstrated. Any of these three relays will be detected as faulty, if the

measured capacitance (Figure A.14) does not change by a margin of 10 pF Table A.3) after the relay is switched.

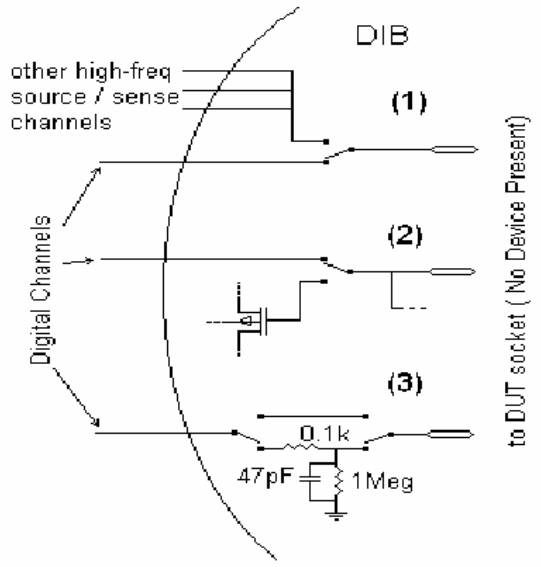

Figure A.13. Experimental setup for detecting continuity fault in different relays

```
Device: 7        Station: 1   Site: 0

Sequencer:  SSimOpenFault
Opening relays: K2, K4, & (K19, K97) ...
 10000 K2 Open            TRelayFault   0.00 pF <    41.89 pF
 10001 K4 Open            TRelayFault   0.00 pF <    61.39 pF
 10002 K19,K97 Open       TRelayFault   0.00 pF <    43.53 pF
Closing relays: K2, K4, & (K19, K97) ...
 10003 K2 Closed          TRelayFault   0.00 pF <    57.85 pF
 10004 K4 Closed          TRelayFault   0.00 pF <   137.87 pF
 10005 K19,K97 Closed     TRelayFault   0.00 pF <    66.35 pF
Bin:  1
```

Figure A.14. Experimental results for detecting switching fault in different relays

For the 3rd relay, there exists a DC path to GND through a large resistor in one of the two switched in electrical paths. It indicates that the capacitance measured in the 'closed' position may not be accurate. However, the technique can still be used for

detecting the switching fault of this relay since the difference in measured capacitance is not within the precision of the measurement.

Table A.3. Measurement of the stray capacitance of the socket pins of a micro-BGA test socket

	Cap. with relay 'open' position pF	Cap. with relay 'closed' position pF	Difference in the measured Cap. pF
1	41.89	57.85	15.96
2	61.39	137.87	76.48
3	43.53	66.35	22.82

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